TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TCM8230MD (A)

TENTATIVE

VGA CAMERA MODULE

The TCM8230MD(A) is a camera module which includes area color image sensor embedded with camera signal processor that meets with VGA format. In the sensor area 492 vertical and 660 horizontal signal pixels, and the image size meets with 1/6 inch optical Format. Use of the CMOS process enables low power consumption operations. It also provides excellent color reproduction through its primary color filter, and embedded camera signal processor enables small and simple camera system. And this module can be assembled by the socket which is suitable for the reflow soldering. So it is fit to use as an image input device for digital still cameras, PC cameras and mobile devices.

Features

1. General

- Module size : 6(W) x 6(D) x 4.5(H) mm
- I^2C BUS I/F
- Sleep mode operation (It can be controlled by the I^2C Bus command)
- Power supply : 2.8+/-0.2V or 2.5+/-0.2V (Sensor(photo diode), I/O) and 1.5+/-0.1V(Sensor(A/D converter), Digital)

2. Sensor

- Optical size : 1/6 inch optical format
- Total pixel numbers : 698(H)x502(V)
- Signal pixel numbers : 660(H)x492(V)
- Pixel pitch : 3.75um(H)x3.75um(V) (square pixel)
- Color filter : RGB color filter, Bayer arrangement (GR line and GB line are arranged alternately.)
- Frame rate : Max 30fps
- Raw data bit precision : 10bit
- Feed back clamp

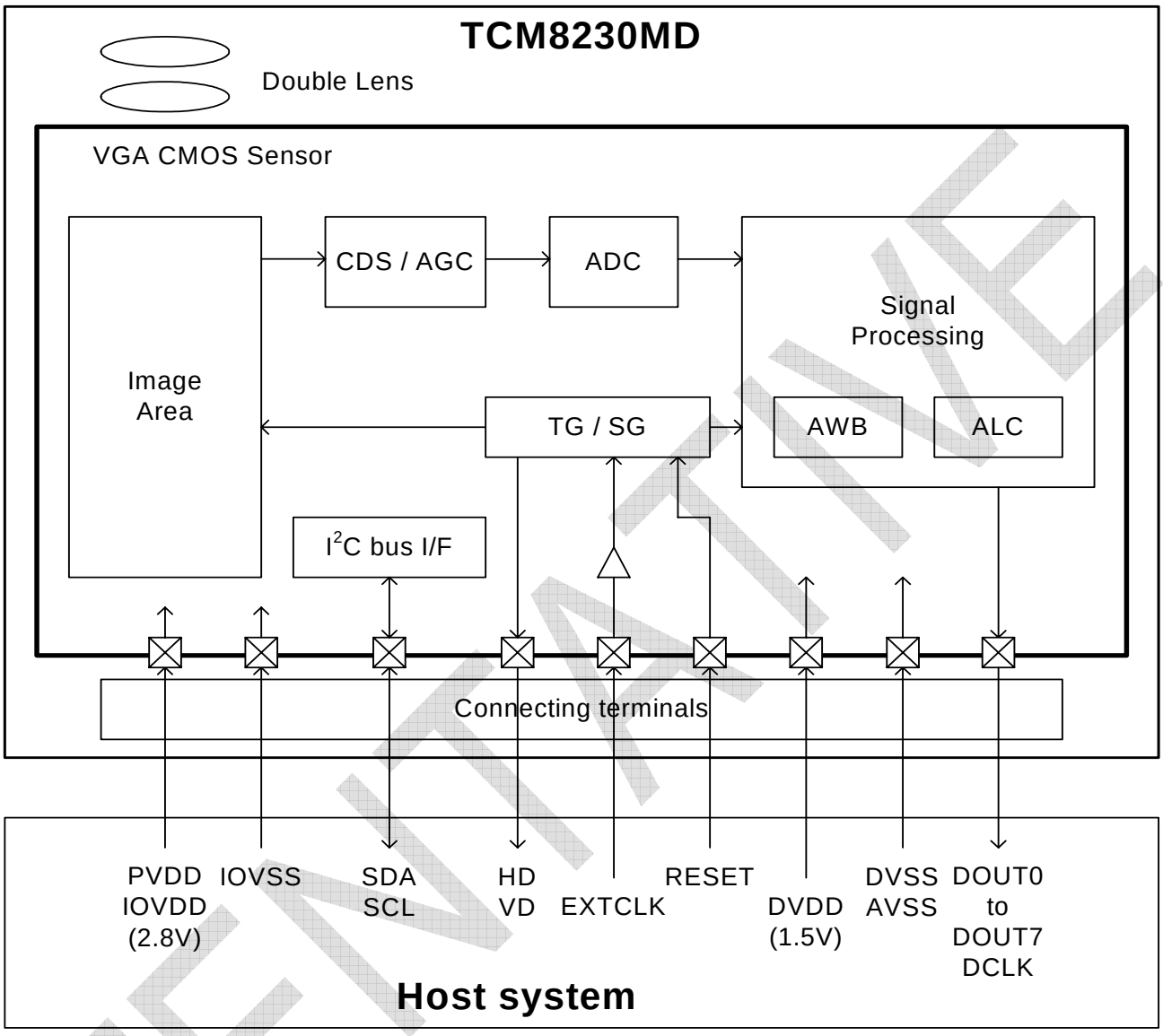
3. Camera signal processing

- Maximum exposure time can be adjust from 1V to 15V
- Digital outputs
  YUV=4:2:2 or RGB=5:6:5 (8bit parallel output)
- Picture size
  VGA, QVGA, QQVGA, CIF, QCIF, subQCIF (Sub-sampling , Windowing)
- Readout internal parameters
  Sensor gain setting, Electrical shutter exposure period, ALC and AWB reference value
- Auto electrical shutter control (AES), auto gain control (AGC) and auto white balance (AWB) circuit
- Flickerless auto luminance control (ALC=AES+AGC) and auto flicker detection circuit for AC 50Hz / 60Hz fluorescent light
- Automatically blemish correction
- Vertical and Horizontal flip mode

UPDATE INFORMATION

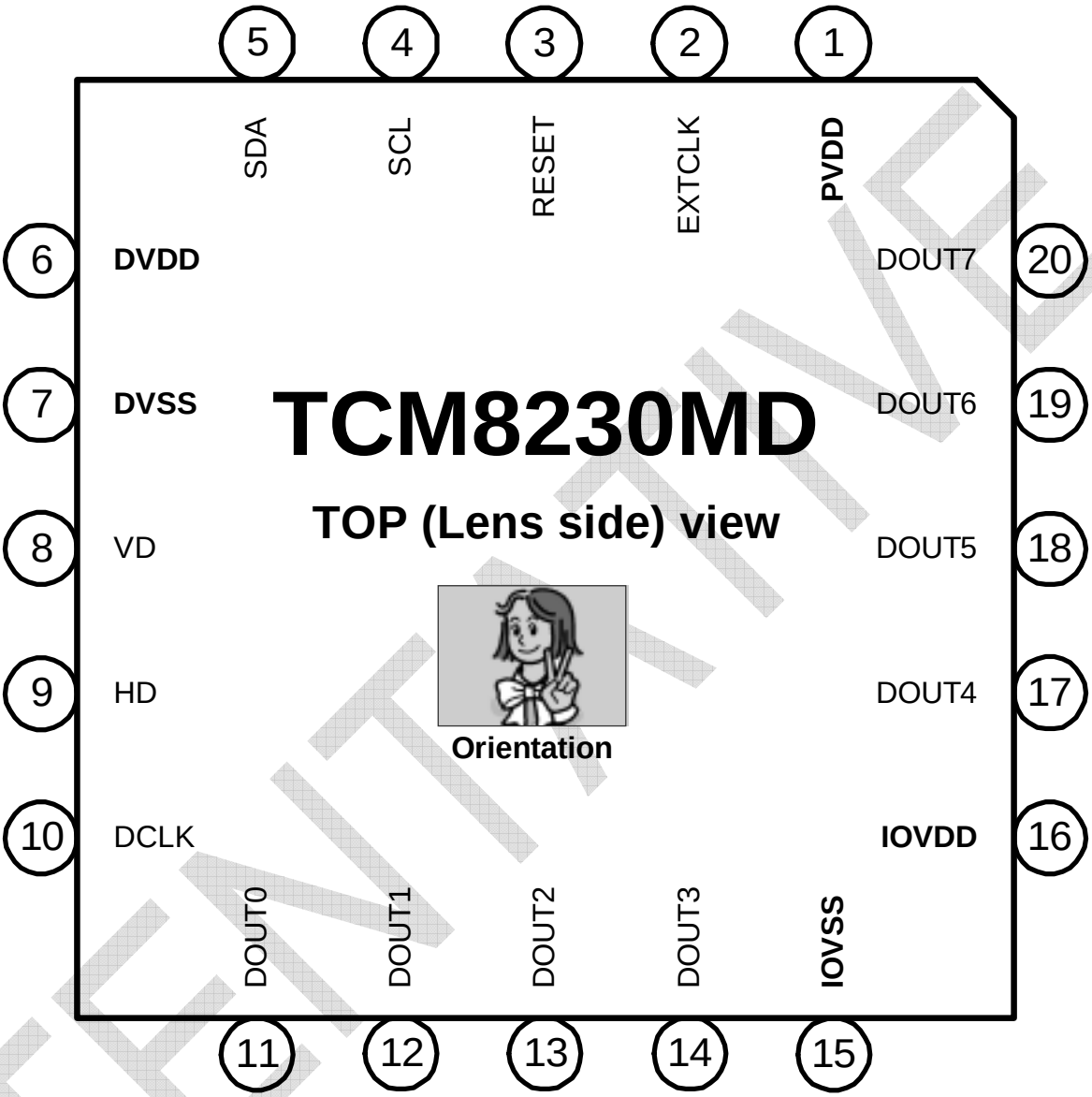
Ver. 1.20 Jan-05, 2004
Ver. 1.10 Dec-23, 2003
Ver. 1.09 Dec-16, 2003
Ver. 1.08 Oct-29, 2003
Ver. 1.07 Oct-07, 2003
Ver. 1.06 Sep-19, 2003
Ver. 1.05 Sep-08, 2003
Ver. 1.04 Aug-11, 2003
Ver. 1.03 Jul-31, 2003
Ver. 1.02 Jul-16, 2003
Ver. 1.01 Jul-03, 2003
Ver. 1.00 Jun-25, 2003

BLOCK DIAGRAM



CDS : Correlated Double Sampling
AGC : Automatic Gain Control
ADC : Analog to Degital Converter
TG : Timing pulse Generator
SG : Sync pulse Generator
AWB : Auto White Balance
ALC : Auto Luminance Control

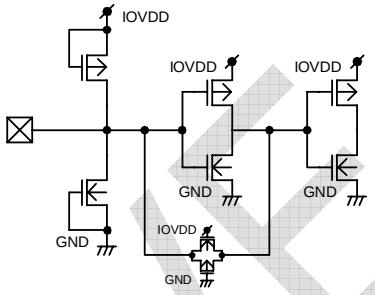
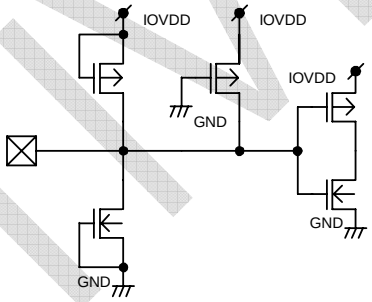
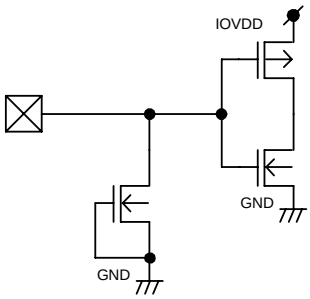
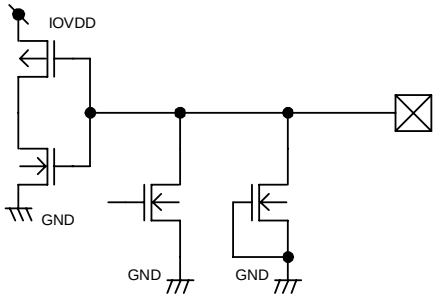
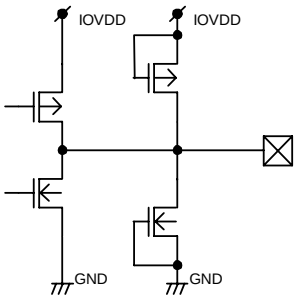
PIN LAYOUT



PIN FUNCTIONS

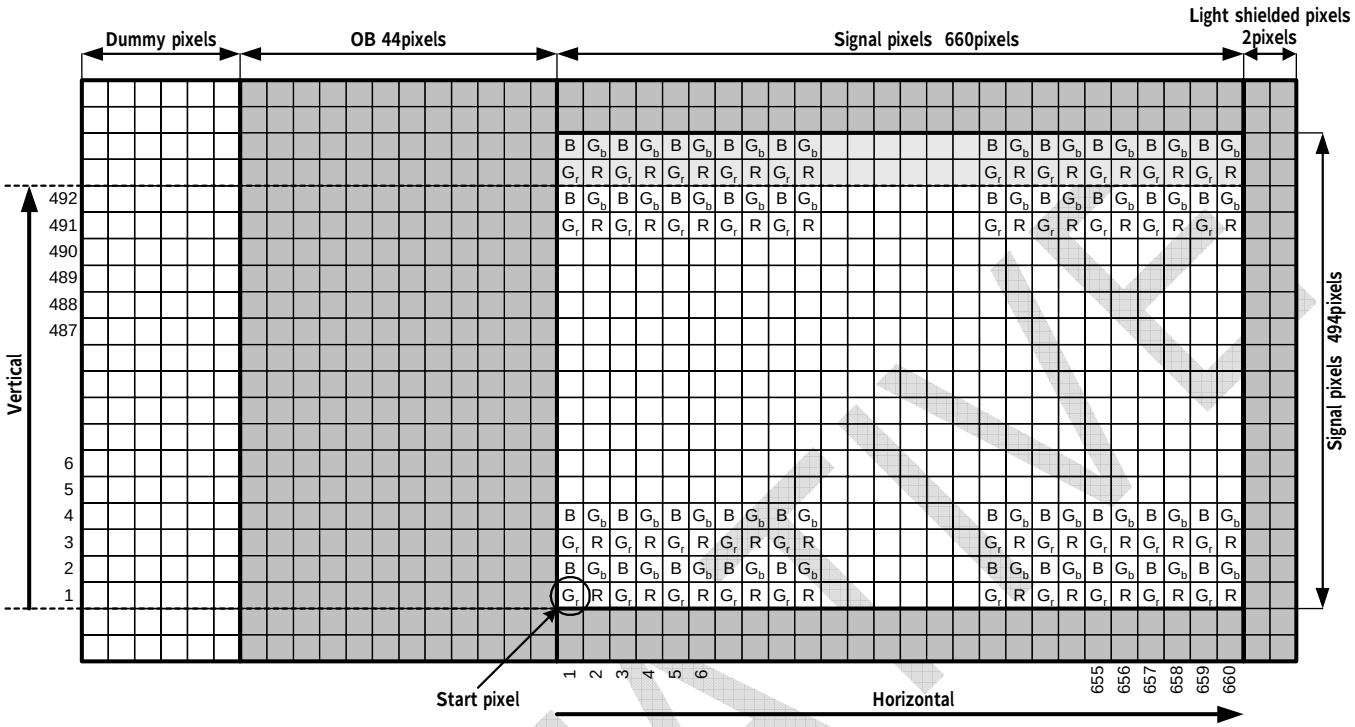
No.	NAME	I/O	FUNCTION
1	PVDD	-	VDD for sensor (photo diode) (2.8V)
2	EXTCLK	I	Clock for external input
3	RESET	I	RESET terminal ("L" active)
4	SCL	I	Clock for I^2C-bus command
5	SDA	I/O	Data for I^2C-bus command
6	DVDD	-	VDD for digital circuits, (1.5V) VDD for sensor (A/D converter) (1.5V)
7	DVSS	-	GND for digital circuits GND for sensor (A/D converter) GND for sensor (photo diode)
8	VD	O	Vertical syncronization pulse output
9	HD	O	Holizontal syncronization pulse output
10	DCLK	O	Clock for output data
11	DOUT0	O	Data output (LSB)
12	DOUT1	O	Data output
13	DOUT2	O	Data output
14	DOUT3	O	Data output
15	IOVSS	-	GND for I/O
16	IOVDD	-	VDD for I/O (2.8V)
17	DOUT4	O	Data output
18	DOUT5	O	Data output
19	DOUT6	O	Data output
20	DOUT7	O	Data output (MSB)

INTERFACE CIRCUITS

PIN No.	NAME	I/O	INTERFACE CIRCUIT
2	EXTCLK	I	
3	RESET ("L" active)	I	
4	SCL	I	
5	SDA	I/O	
8-14, 17-20	DOUT0 to DOUT7, HD, VD, DCLK	O	

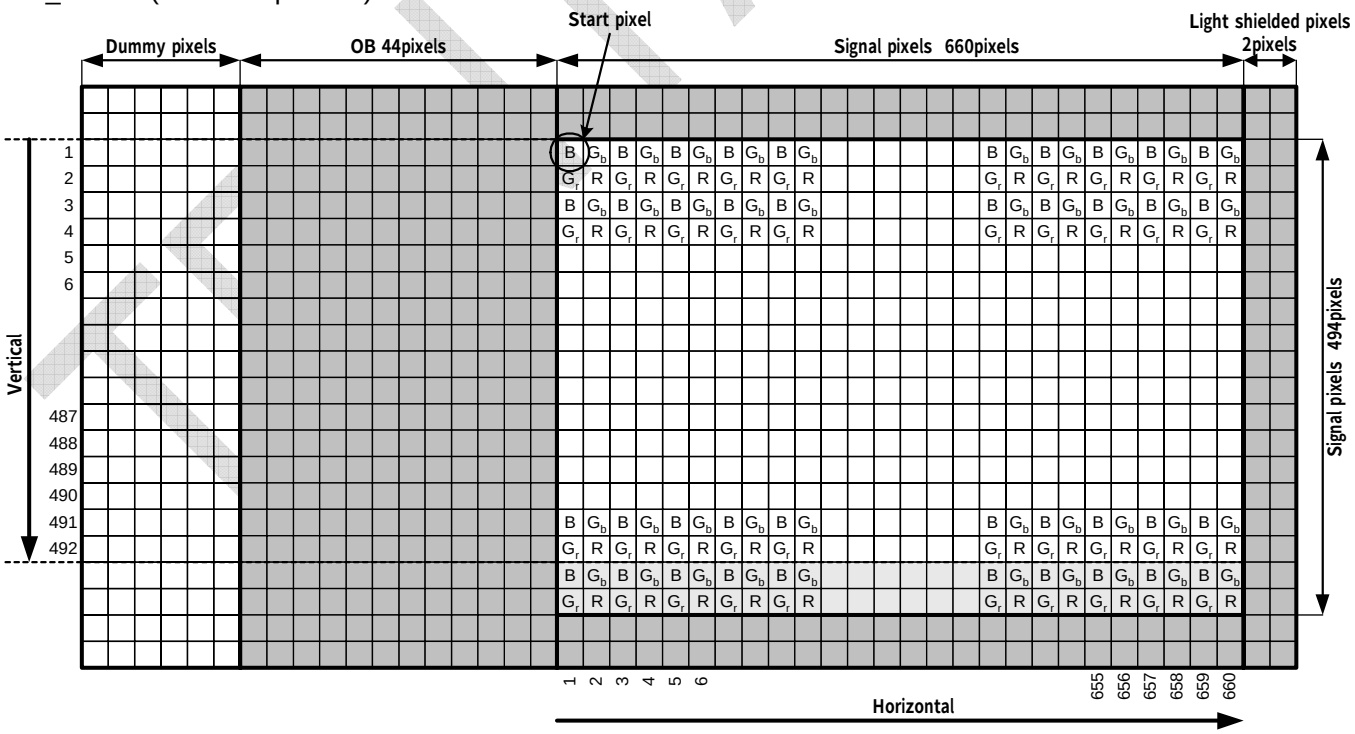
PIXEL ARRANGEMENT

1. V_INV=0



OB: Optical Black R: Red pixels Gr,Gb: Green pixels B: Blue pixels

2. V_INV =1 (Vertical flip mode)

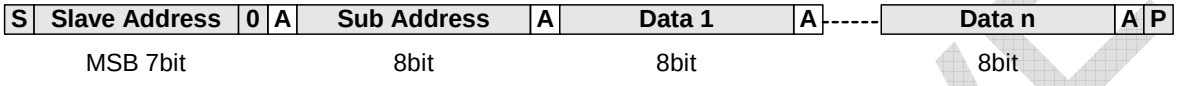


OB: Optical Black R: Red pixels Gr,Gb: Green pixels B: Blue pixels

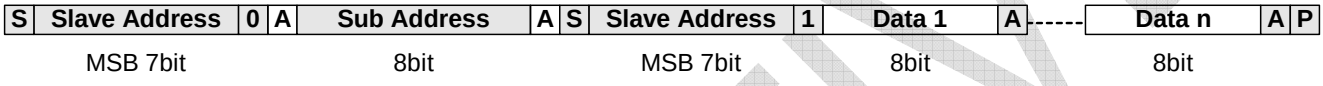
CONTROL I/F

TCM8230MD(A) control interface configuration is based on fast mode I^2C bus.
Register setting can be changed via I^2C bus.
All register settings are able to read via I^2C bus.

Write mode



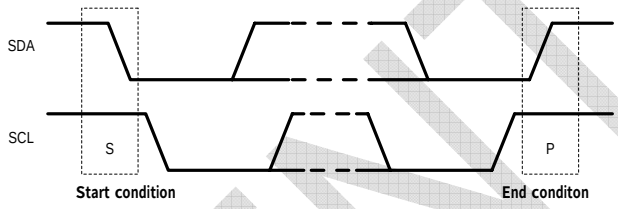
Read mode



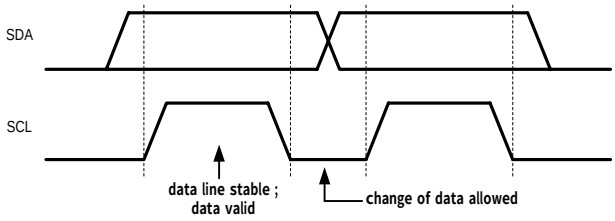
: Host Command
: TCM8230MD(A)

S : Start condition
P : End condition
A : Acknowledge

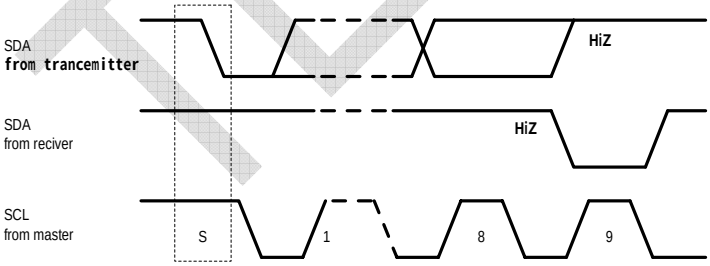
Start condition, End condition



Bit Transfer



Acknowledge



Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	1	1	1	0	0	1/0

* TCM8230MD(A) use 7bit Slave address

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

INTERNAL REGISTER

ADDRESS			fast							last	default(ROM data)								
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX
0	00000000	00									0	1	1	1	0	0	0	0	70
1	00000001	01	**Test Mode**								0	0	0	1	0	0	0	0	10
2	00000010	02	**FPS** 0:30fps 1:15fps	**ACF** 0:50Hz 1:60Hz					**DCLKP** 0 : normal 1: reverse	**ACFDET** 0 : AUTO 1: MANUAL	1	1	0	0	0	0	0	0	40
3	00000011	03	**DOUTSW** 0:ON 1:0FF	**DATAHZ** 0:OUT 1:Hi-Z	**PICSIZ**[3:0] 0h:VGA 1h:QVGA(f) 2h:QVGA(z) 3h:QQVGA(f) 4h:QQVGA(z) 5h:CIF(f) 6h:QCIF(f) 7h:QCIF(z) 8h:subQCIF(f) 9h:subQCIF(z)				**PICFMT** 0:YUV422 1:RGB565	**CM** 0:COLOR 1:B/W	1	0	0	0	0	0	0	0	80
4	00000100	04	**V_INV** 0:normal 1:invert	**H_INV** 0:normal 1:invert	**ESRLSW[1:0]** 0h : Short 1h : Long 2h & 3h :		**V_LENGTH**[3:0]				0	0	0	0	1	1	1	1	0F
5	00000101	05	**ALCSW** 0:AUTO 1:MANUAL	**ESRLIM**[1:0]		**ESRSPD**[12:8]					0	0	0	0	0	0	1	0	02
6	00000110	06	**ESRSPD**[7:0]								0	0	0	0	1	1	0	1	0D
7	00000111	07	**AG**[7:0]								1	1	0	0	0	0	0	0	C0
8	00001000	08			**ALCMODE**[1:0] 0h:Centaer Weight 1h:Average 2h:Center only 3h:Backlight		**ALCH**[3:0]				0	0	1	1	1	0	0	0	38
9	00001001	09	**ALCL**[7:0]								0	1	0	0	0	0	0	0	40
10	00001010	0A	**AWBSW** 0:AUTO 1:MANUAL								0	0	0	0	0	0	0	0	00
11	00001011	0B	**MRG**[7:0]								0	1	0	0	0	0	0	0	40
12	00001100	0C	**MBG**[7:0]								0	1	0	0	0	0	0	0	40
13	00001101	0D	**GAMSW** 0:ON 1:OFF								0	0	0	0	0	0	0	0	00
14	00001110	0E	**HDTG**[7:0]								0	0	1	0	1	1	1	1	2F
15	00001111	0F	**VDTG**[7:0]								0	0	0	0	0	1	0	0	04
16	00010000	10	**HDTCORE**[3:0]				**VDTCORE**[3:0]				0	0	1	0	0	0	1	0	22
17	00010001	11	**CONT**[7:0]								1	0	0	1	1	0	1	0	9A
18	00010010	12	**BRIGHT**[7:0]								0	0	0	0	1	1	0	0	0C
19	00010011	13		**VHUE**[6:0]							0	0	0	0	1	0	1	0	0A
20	00010100	14		**UHUE**[6:0]							0	0	0	0	1	0	0	0	08
21	00010101	15			**VGAIN**[5:0]						0	0	1	1	1	0	0	0	38
22	00010110	16			**UGAIN**[5:0]						0	0	1	1	1	0	0	0	38
23	00010111	17					**UVCORE**[3:0]				0	0	0	0	0	0	0	1	01
24	00011000	18		**SATU**[6:0]							0	0	1	0	0	1	1	1	27
25	00011001	19	**MHMODE** 0: 1:	**MHLPFSEL** 0: 1:	**YMODE**[1:0]			**MIXHG**[2:0]			0	0	0	0	0	1	0	0	04
26	00011010	1A			**LENS**[5:0]						0	0	1	0	0	0	0	0	20
27	00011011	1B	**AGLIM**[2:0]			**LENSRPOL** 0:Gain up 1:Gain down	**LENSRGAIN**[3:0]				0	1	0	0	0	1	1	0	46
28	00011100	1C	**ES100S**[7:0]								1	0	0	1	1	1	1	0	9E
29	00011101	1D	**ES120S**[7:0]								1	0	0	0	0	0	1	1	83
30	00011110	1E	**D_MASK**[1:0]		**CODESW** 0:OFF 1:OUT	**CODESEL** 0 : original 1 : ITU656	**HSYNCSEL** 0 : normal 1 :	**TESPIC** 0:Not out 1:Out	**PICSEL**[1:0] 0h:Colorbar 1h:Ramp1 2h :Ramp2		0	1	1	0	1	0	0	0	68
31	00011111	1F	**SLEEPSW** 0:ACTIVE 1:SLEEP	**SRST** 0:OFF 1:reset							0	0	0	0	0	0	0	0	00

The registers of gray mesh (unassigned registers) are not defined. Input data of the registers of gray mesh must input “0”. The registers of testmode must input default data.

ADDRESS			fast							last	default								
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX
32	00100000	20	**HNUM**[7:0]								0	0	0	0	0	0	0	0	**00**
33	00100001	21	**HPPH**[7:0]								0	0	0	0	0	0	0	1	**01**
34	00100010	22	**HPPH**[8]	**VRRPH**[6:0]							0	0	1	0	0	1	1	0	**26**
35	00100011	23	**HDSPPH**[7:0]								0	1	0	0	0	0	0	0	**40**
36	00100100	24	**HDSPPH**[8]	**VDSPPH**[6:0]							0	0	1	0	0	1	1	1	**27**
37	00100101	25	**HAPRPH**[7:0]								0	1	0	1	1	1	1	1	**5F**
38	00100110	26	**HAPRPH**[8]								0	0	0	0	0	0	0	0	**00**
39	00100111	27	**HOUTPH**[7:0]								0	0	0	1	0	1	1	0	**16**
40	00101000	28	**HOUTPH**[8]	**VOUTPH**[6:0]							0	0	1	0	0	0	1	1	**23**
41	00101001	29	**FSSTBSW** 0 : NOT OUT 1 : OUT	**FSSTBPOL** 0 : normal 1 : invert			**FSSTBPH[3:0]**				0	0	0	0	1	0	0	0	**08**
42	00101010	2A					**FSSTBW[3:0]**				0	0	0	0	1	0	0	0	**08**
43	00101011	2B					**SCMD[19:16]**				0	0	0	0	0	1	0	0	**04**
44	00101100	2C	**SCMD[15:8]**								0	0	0	0	0	0	0	0	**00**
45	00101101	2D	**SCMD[7:0]**								0	0	0	0	0	0	0	0	**00**
46	00101110	2E	**TCSB1L** 0: 1:	**TCPEROSW** [2:0]			**TCSBIN** 0: 1:	**TCRAM** 0: 1:	**TROM[1:0]**		0	0	0	0	0	0	0	0	**00**
47	00101111	2F	**TCRAMS** 0: 1:	**TSPCHK** 0: 1:	**TCPERAGC**	**TALCRST**	**TWBS**	**TWBG**	**TACDET**[1:0]		0	0	0	0	0	0	0	0	**00**
48	00110000	30		**TGAMROM** 0: 1:			**TCSB[3:0]**				0	0	0	0	0	0	0	0	**00**
49	00110001	31	**TALCDISP** 0: 1:	**TALCOSW**[2:0]			**PBDISP**[1:0]		**TDISP**[1:0]		0	0	0	0	0	0	0	0	**00**
50	00110010	32		**ESROUT**[14:8]							0	0	0	0	0	0	0	0	**00**
51	00110011	33	**ESROUT**[7:0]								0	0	0	0	0	0	0	0	**00**
52	00110100	34	**AGOUT**[7:0]								0	0	0	0	0	0	0	0	**00**
53	00110101	35		**DGOUT**[5:0]							0	0	0	0	0	0	0	0	**00**
54	00110110	36	**ALCDATA**[7:0]								0	0	0	0	0	0	0	0	**00**
55	00110111	37	**AWBRYDA**[7:0]								0	0	0	0	0	0	0	0	**00**
56	00111000	38	**AWBBYDA**[7:0]								0	0	0	0	0	0	0	0	**00**
57	00111001	39	**AGSLOW1**[1:0]	**FLLSMODE**[1:0]			**FLLSLIM**[3:0]				1	0	0	0	1	1	0	0	**8C**
58	00111010	3A	**DETSEL**[3:0]				**ACDETNC**[3:0]				1	1	0	0	1	1	1	1	**CF**
59	00111011	3B	**AGSLOW2**[1:0]	**DG**[5:0]							1	0	0	0	0	0	0	0	**80**
60	00111100	3C	**REJHLEV**[7:0]								0	0	0	0	0	0	0	0	**00**
61	00111101	3D	**ALCLOCK** 0: 1:	**FPSLNRSW** 0: 1:	**ALCSPD[1:0]**		**ALCSTEP[1:0]**		**REJH**[1:0]		0	0	0	1	0	1	1	1	**17**
62	00111110	3E	**SHESRSW** 0:Disable 1:Enable	**ESLIMSEL** 0: 1:	**SHESRSPD**[1:0]		**ELSTEP**[1:0]		**ELSTART**[1:0]		1	0	0	0	0	1	0	1	**85**
63	00111111	3F	**AGMIN**[7:0]								1	1	0	0	0	0	0	0	**C0**

The registers of gray mesh (unassigned registers) are not defined. Input data of the registers of gray mesh must input “0”. The registers of testmode must input default data.

ADDRESS			fast							last	default								
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX
64	01000000	40	**LI1POL** 0: 1:	**CS1POL** 0: 1:	**LI3POL** 0: 1:	**CS3POL** 0: 1:				**DINCKSW** 0: 1:	0	0	0	0	0	0	0	0	**00**
65	01000001	41	**JAMP** 0: 1:	**JAMG**[6:0]							0	0	0	0	0	0	0	0	**00**
66	01000010	42		**PREGRG**[5:0]							0	0	0	0	0	0	0	0	**00**
67	01000011	43		**PREGBG**[5:0]							0	0	0	0	0	0	0	0	**00**
68	01000100	44		**PRERG**[5:0]							0	0	0	1	0	1	0	1	**15**
69	01000101	45		**PREBG**[5:0]							0	0	0	1	1	1	1	1	**1F**
70	01000110	46									0	0	0	0	0	0	0	0	**00**
71	01000111	47		**MSKBR**[6:0]							0	1	0	0	0	1	0	0	**44**
72	01001000	48		**MSKGR**[6:0]							0	1	0	0	0	1	0	0	**44**
73	01001001	49		**MSKRB**[6:0]							0	0	1	0	0	0	0	0	**20**
74	01001010	4A		**MSKGB**[6:0]							0	1	0	0	0	1	0	1	**45**
75	01001011	4B		**MSKRG**[6:0]							0	1	1	0	0	1	1	0	**66**
76	01001100	4C		**MSKBG**[6:0]							0	0	1	1	0	0	0	0	**30**
77	01001101	4D	**HDTCSW** 0: 1:	**VDTCSW** 0: 1:	**DTCYLV**[5:0]						1	1	1	0	0	0	0	0	**E0**
78	01001110	4E	**HDTPSW** 0: 1:	**VDTPSW** 0: 1:	**DTCGAIN**[5:0]						0	0	1	0	0	0	0	0	**20**
79	01001111	4F	**LI12POL** 0: 1:	**CS12POL** 0: 1:		**DTLLIMSW** 0: 1:	**DTLYLIM** [3:0]				0	0	0	0	1	0	0	1	**09**
80	01010000	50	**YLCUTLMSK** 0: 1:		**YLCUTL**[5:0]						0	0	0	0	0	1	1	1	**07**
81	01010001	51	**YLCUTHMSK** 0: 1:		**YLCUTH**[5:0]						0	0	1	0	1	1	1	1	**2F**
82	01010010	52		**UVSKNC**[6:0]							0	0	0	0	0	0	1	0	**02**
83	01010011	53		**UVLJ**[6:0]							0	0	0	0	0	0	0	0	**00**
84	01010100	54	**WBGMIN**[7:0]								0	0	1	0	1	0	1	1	**2B**
85	01010101	55	**WBGMAX**[7:0]								0	1	1	0	0	0	0	0	**60**
86	01010110	56	**AWBCSPOLE** 0:	**WBDIVCLP** 0: 1:	**WBNOLJ**[1:0]		**WBNOLJSC** 0: 1:	**WB2IM1** 0: 1:	**WBSPDUP**[1:0]		0	1	0	0	0	0	0	0	**40**
87	01010111	57						**WBDIVSC**[2:0]			0	0	0	0	0	1	1	0	**06**
88	01011000	58			**ALLAREA** 0: 1:	**WBLOCK** 0: 1:	**WB2SP** [3:0]				0	0	1	0	0	0	1	0	**22**
89	01011001	59			**KIZUSW** 0:OFF 1:ON	**PBRDSW**			**ABCSW**[1:0]		0	0	1	0	0	0	1	1	**23**
90	01011010	5A	**PBDLV**[7:0]								0	0	0	0	1	0	0	0	**08**
91	01011011	5B	**PBC1LV**[7:0]								0	0	0	0	0	1	0	0	**04**
92	01011100	5C	**PBC2LV**[7:0]								0	0	0	0	1	0	0	0	**08**
93	01011101	5D	**PBC3LV**[7:0]								0	0	0	0	1	0	0	0	**08**
94	01011110	5E	**PBC4LV**[7:0]								0	0	0	0	1	0	0	0	**08**

The registers of gray mesh (unassigned registers) are not defined. Input data of the registers of gray mesh must input “0”. The registers of testmode must input default data.

OUTLINE OF INTERNAL REGISTER

* Frame rate setting (30fps, 15fps)
* Picture size setting of digital output (VGA, QVGA, QQVGA, CIF, QCIF, subQCIF)
* Selection of digital data output format (8bit YUV422, RGB565)
* Sync. code setting (ON/OFF, 2 mode)
* Color signal adjustment (Masking, color axis correction, saturation, etc.)
* Luminance signal adjustment (Contrast, Brightness, Gamma, H,V edge enhancement)
* ALC ON/OFF
* ALC mode setting (area selection, speed selection, flicker reduction mode setting)
* AWB ON/OFF
* Vertical and Horizontal flip
* Sleep mode setting
* Some kinds of correction setting (Lens shading correction etc.)

8bit parallel image data

	YUV mode				RGB mode	
	1st	2nd	3rd	4th	1st	2nd
DOUT0	U0(n)	Y0(n)	V0(n)	Y0(n+1)	B0	G3
DOUT1	U1(n)	Y1(n)	V1(n)	Y1(n+1)	B1	G4
DOUT2	U2(n)	Y2(n)	V2(n)	Y2(n+1)	B2	G5
DOUT3	U3(n)	Y3(n)	V3(n)	Y3(n+1)	B3	R0
DOUT4	U4(n)	Y4(n)	V4(n)	Y4(n+1)	B4	R1
DOUT5	U5(n)	Y5(n)	V5(n)	Y5(n+1)	G0	R2
DOUT6	U6(n)	Y6(n)	V6(n)	Y6(n+1)	G1	R3
DOUT7	U7(n)	Y7(n)	V7(n)	Y7(n+1)	G2	R4

Image size format

Image size	Display mode	Pixels per H	Effective H lines	Start point (H, V)	End point (H, V)	DCLK mode	Operation mode	Resizing method
VGA	Full	640	480	(1, 1)	(640 ,480)	1	Normal	-
QVGA	Full	320	240	(1, 1)	(639, 479)	1/2	Low power	Sub-sampling from VGA
	Zoom x 2			(161, 121)	(480 ,360)	1	Normal	Windowing from VGA
QQVGA	Full	160	120	(1, 1)	(637, 477)	1/2	Low power	Sub-sampling from QVGA(f)
	Zoom x 2			(161, 121)	(479, 359)			Sub-sampling from VGA
CIF	Full	352	288	(21, 1)	(608, 478)	1	Normal	3/5 filtering from VGA
QCIF	Full	176	144	(21, 1)	(608, 478)	1/2	Low power	3/5 filtering from QVGA(f)
	Zoom x 2			(173, 121)	(466, 360)	1	Normal	Windowing from CIF
subQCIF	Full	128	96	(1, 1)	(636, 476)	1/2	Low Power	4/5 filtering from QQVGA(f)
	Zoom x 2			(161, 121)	(479, 359)			1st: 3/5 filtering from QVGA(f) 2nd: Sub-sampling from "1st"

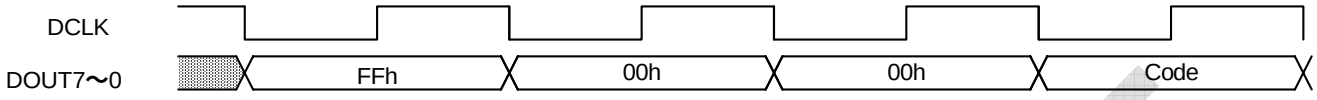
QVGA(f) means QVGA full.
QQVGA(f) means QVGA full.

VGA	Video Graphics Array
QVGA	Quarter VGA
QQVGA	Quarter QVGA
CIF	Common Intermediate Format
QCIF	Quarter CIF

SYNCHRONIZATION CODE

Synchronization code output format

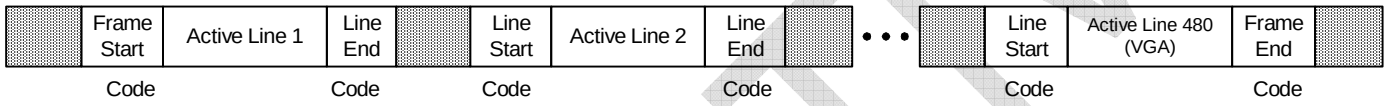
CODESW=1

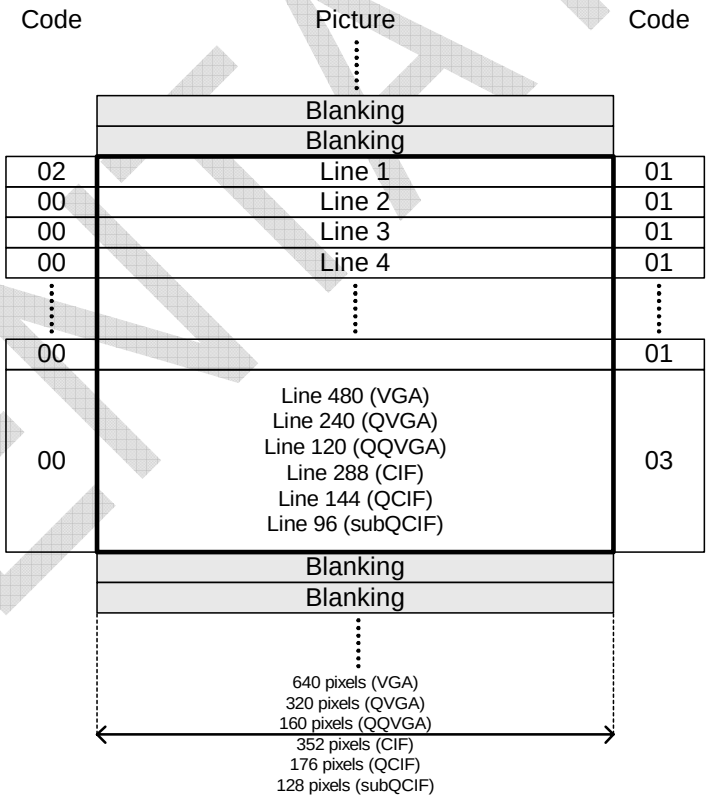


CODESW(Address=1Eh, Bit5) is able to add synchronization codes. “Code“ part is changed Mode1 or Mode2 by CODESEL(Address=1Eh, Bit4).

Mode1 (Original format, CODESEL=0)

These codes only exists in active lines





Line start code : FFh 00h 00h 00h
Line end code : FFh 00h 00h 01h
Frame start code : FFh 00h 00h 02h
Frame end code : FFh 00h 00h 03h

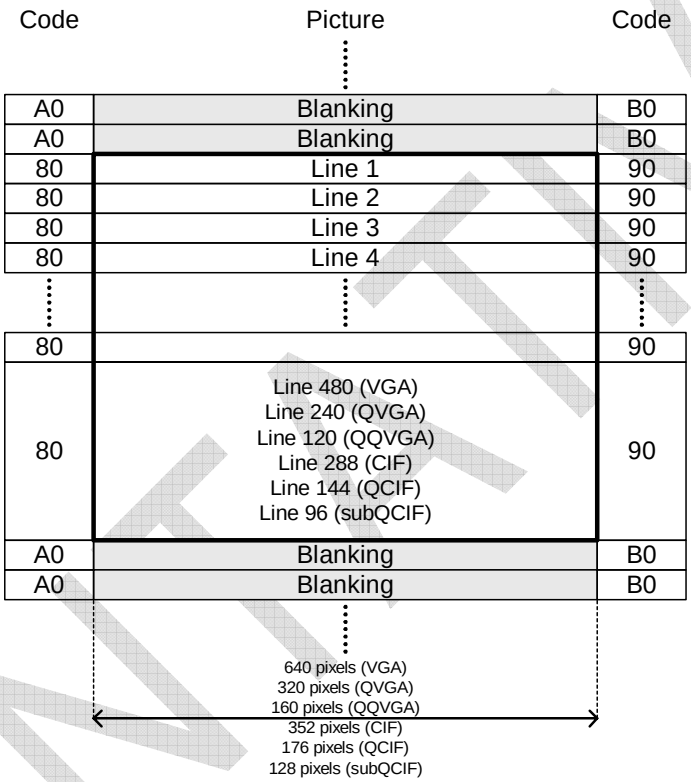
Mode2 (ITU656 format, CODESEL=1)

These codes exists in every lines

Code	1	0	V	H	0	0	0	0

V : 1:Blanking 0:Active Line

H : 1:End of Active Pixel 0:Start of Active Pixel



Blanking and start active pixel code : FFh 00h 00h A0h
Blanking and endactive pixel code : FFh 00h 00h B0h
Active line and start active pixel code : FFh 00h 00h 80h
Active line and end active pixel code : FFh 00h 00h 90h

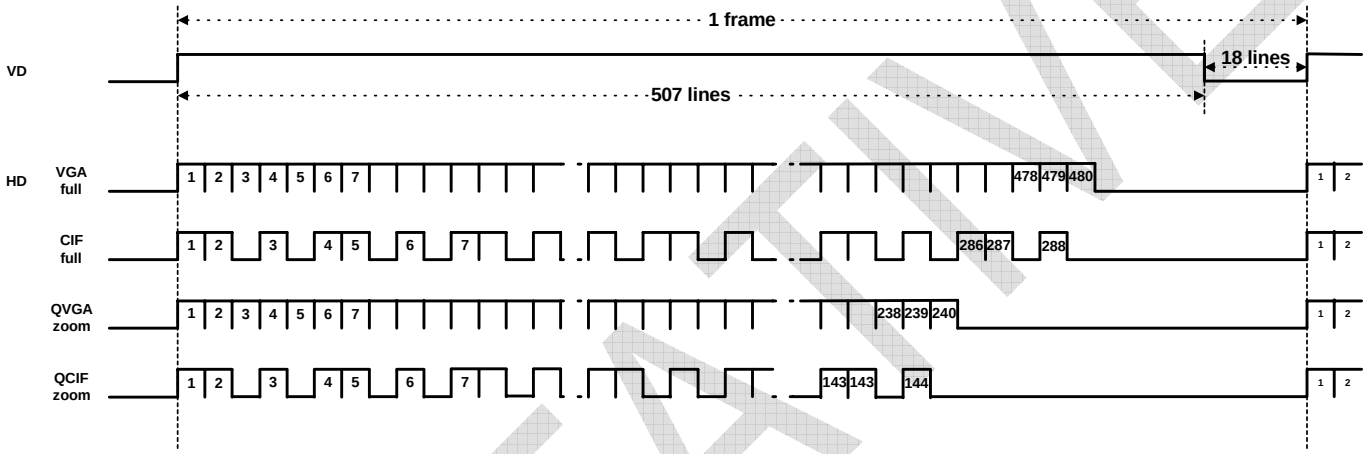
DATA OUTPUT TIMING CHART

TCM8230MD supports 2 HD pulses, one is “Blanking pulse”, and another one is “Normal pulse”.
You can choose HD pulse by HSYNCSEL (Address=1Eh Bit3).

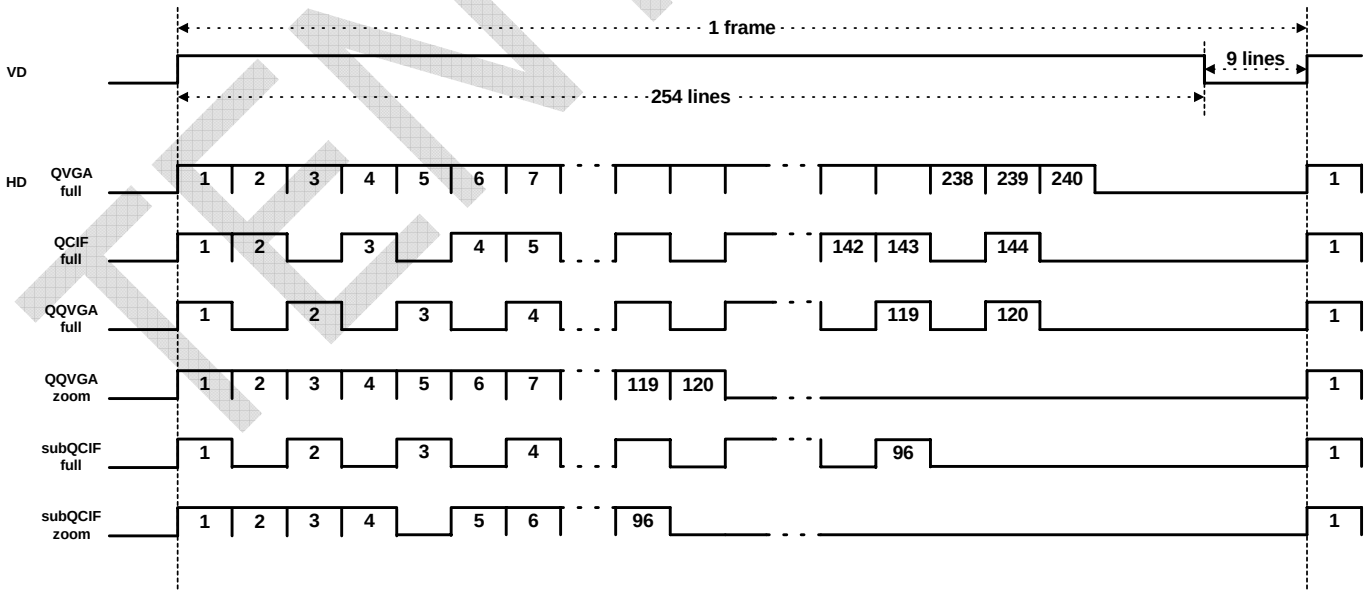
Pixel Size mode (HD=Blanking pulse)

1. Vertical timing (HSYNCSEL=1)

Normal operation mode
(VGA, CIF(full), QVGA(zoom), QCIF(zoom))

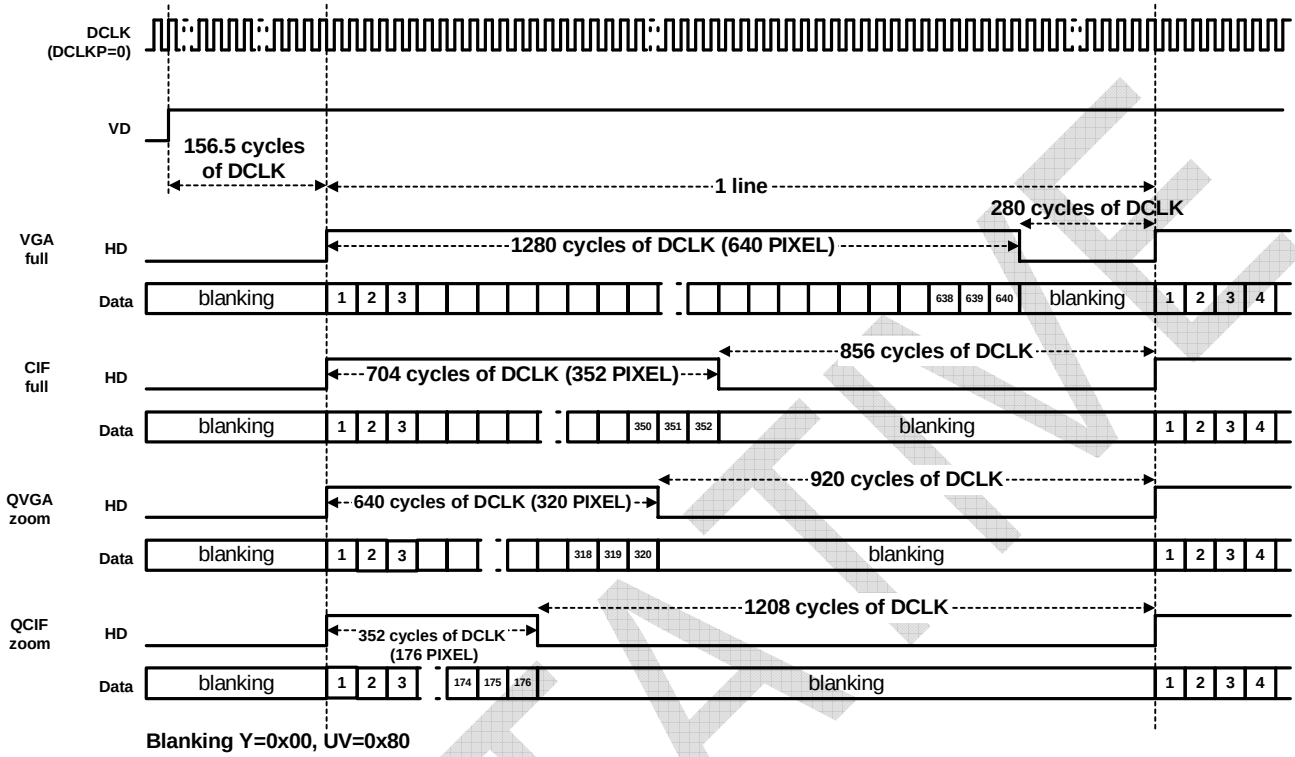


Low power operation mode
(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))



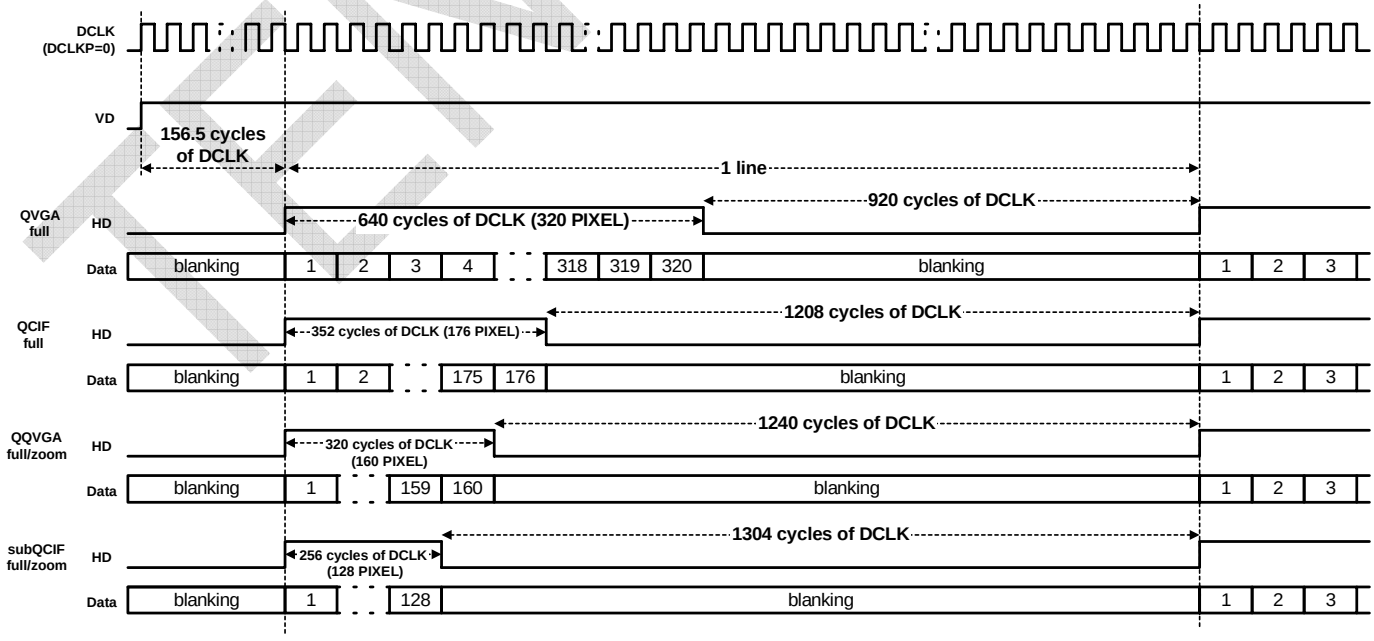
2. Horizontal timing (HSYNCSEL=1)

Normal operation mode
(VGA, CIF (full), QVGA (zoom), QCIF (zoom))



Blanking Y=0x00, UV=0x80
HNUM=0

Low power operation mode
(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))

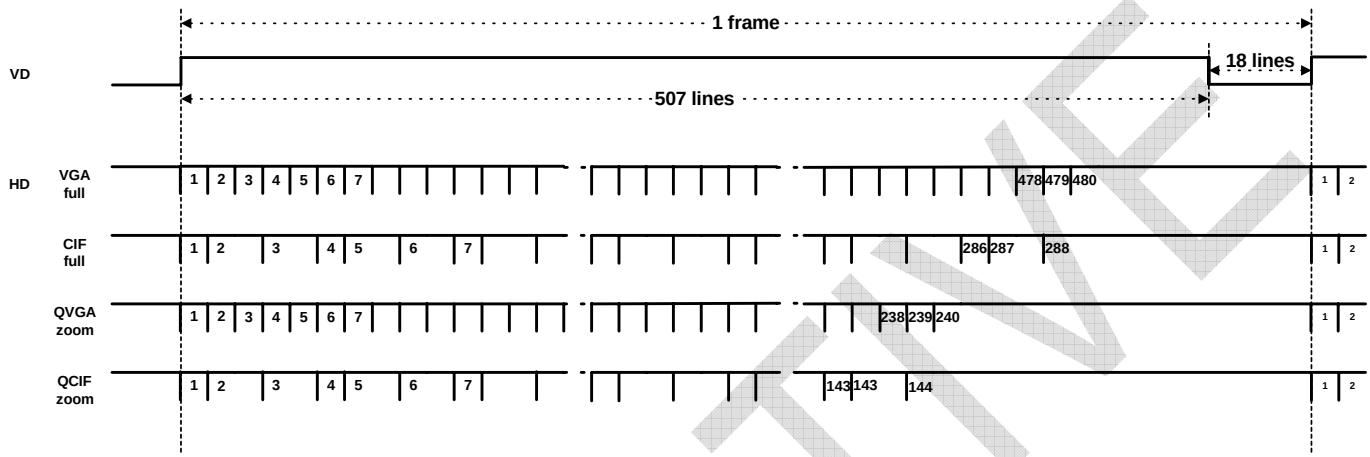


Blanking Y=0x00, UV=0x80

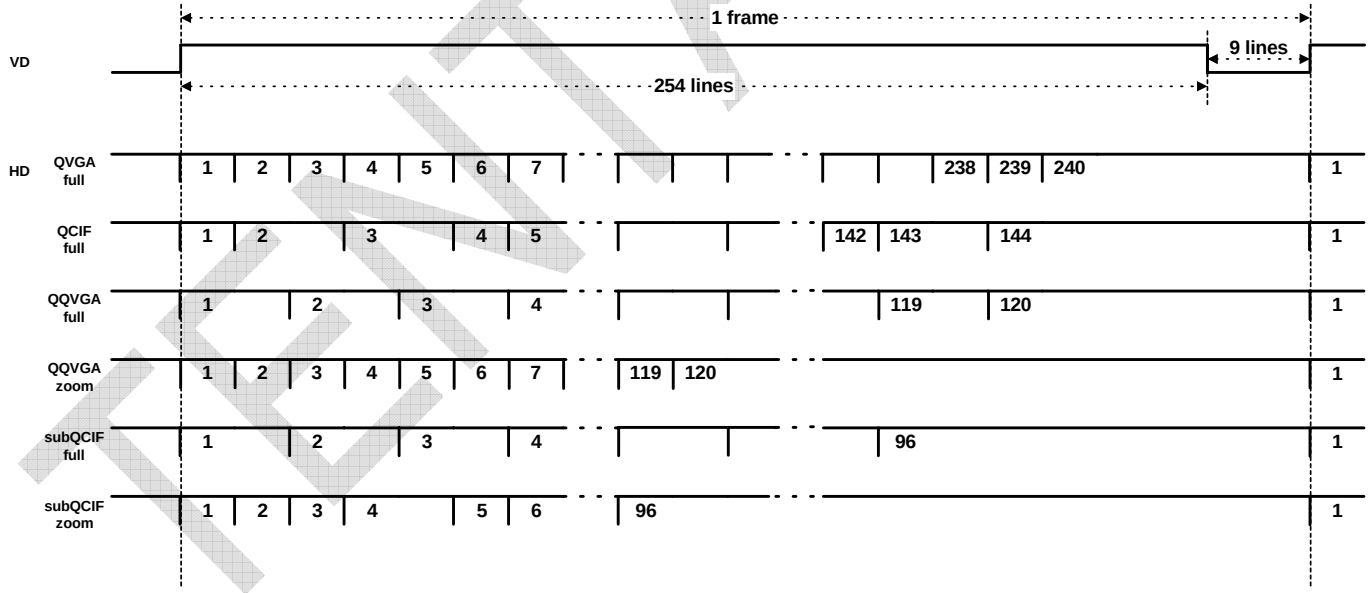
Pixel Size mode (HD=Normal pulse)

1. Vertical timing (HSYNCSEL=0)

Normal operation mode
(VGA, CIF(full), QVGA(zoom), QCIF(zoom))

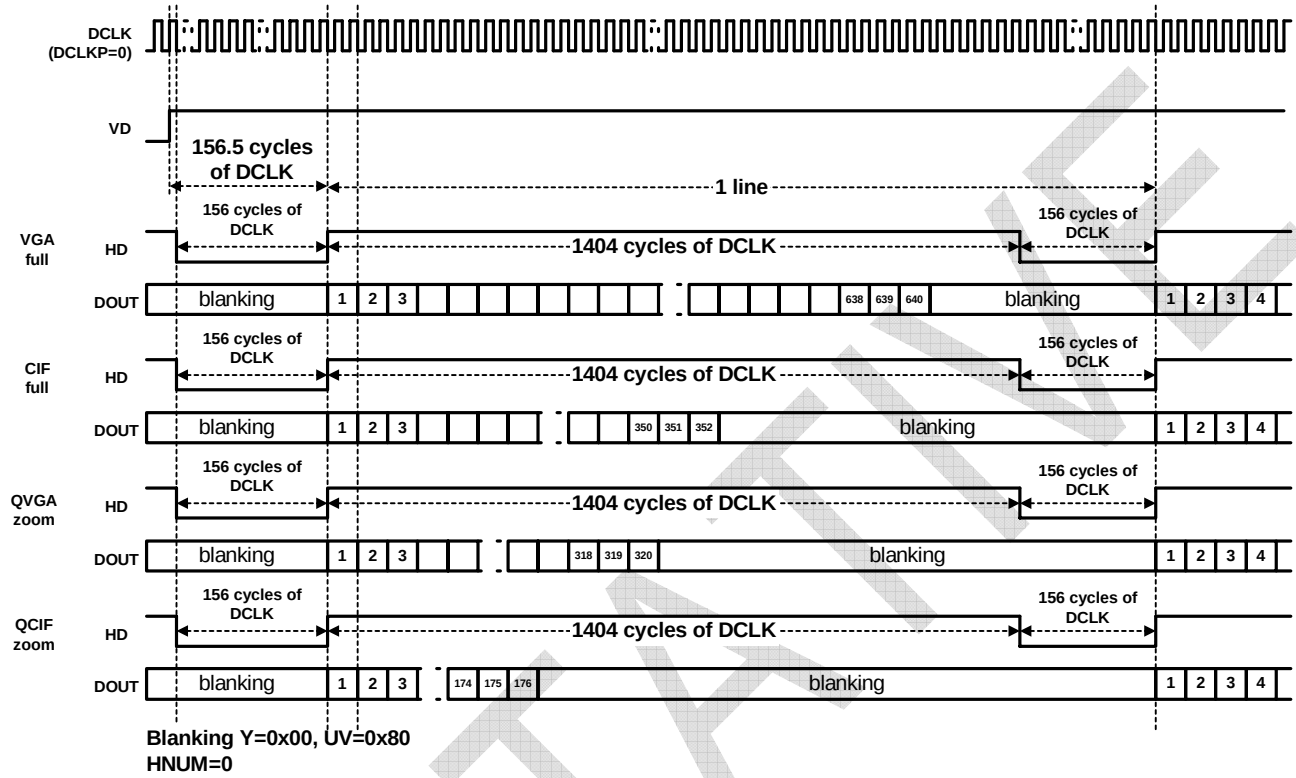


Low power operation mode
(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))

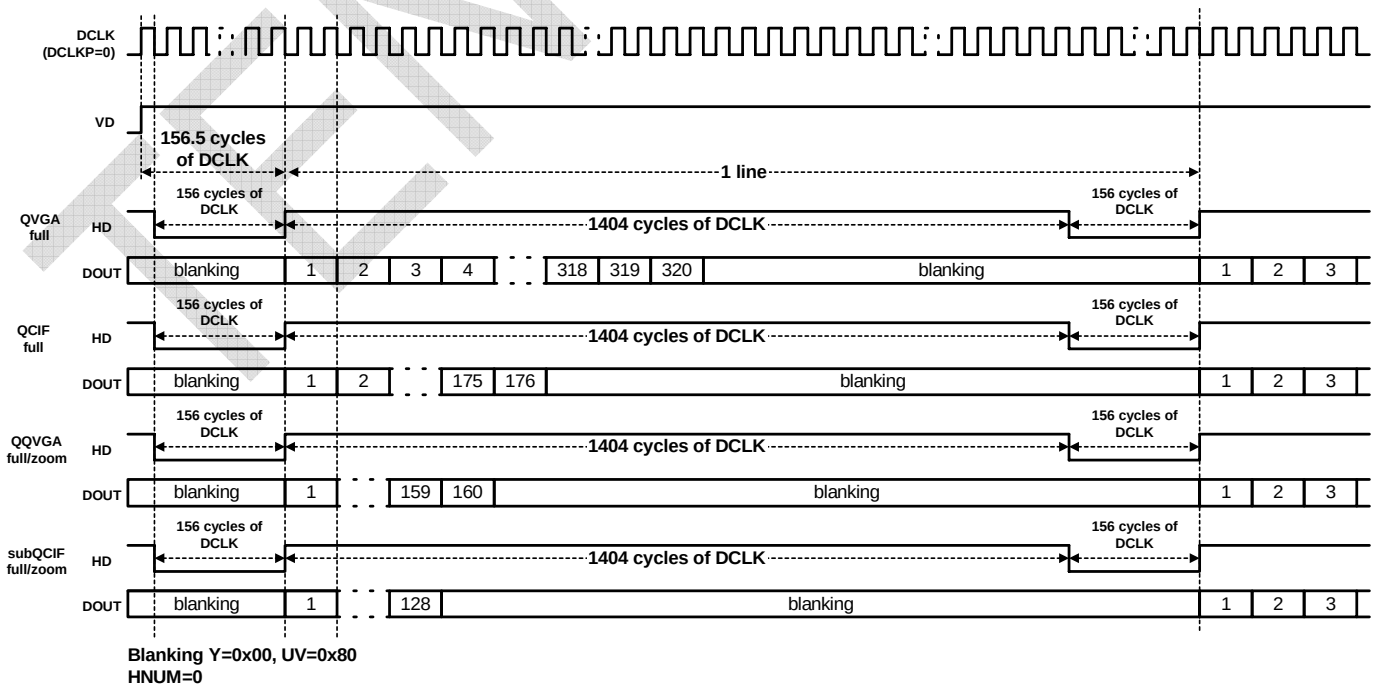


2. Horizontal timing (HSYNCSEL=0)

Normal operation mode
(VGA, CIF (full), QVGA (zoom), QCIF (zoom))



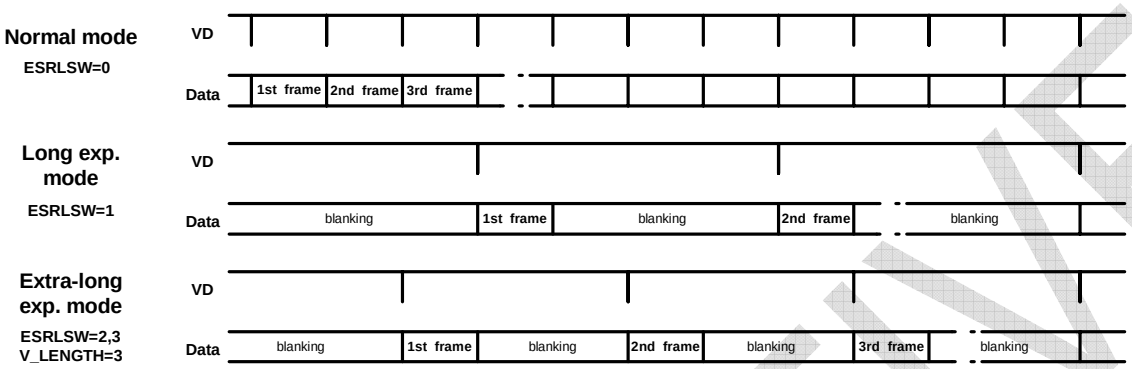
Low power operation mode
(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))



Exposure mode

TCM8230MD supports long exposure time mode (ESRLSW (Address=04h, Bit5,4)= 1) and extra-long exposure time mode (ESRLSW (Address=04h Bit5,4)= 2, 3).

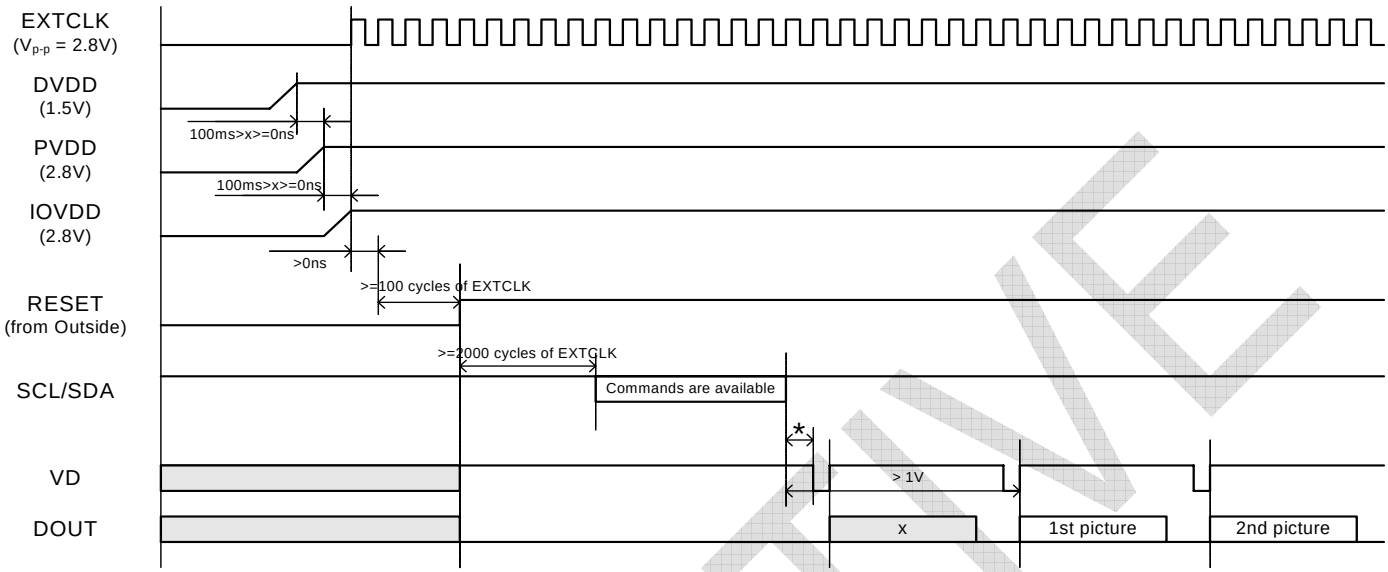
Vertical timing



When use these modes, you should be sent below I^2C commands before entry these modes.

ESRLSW (Address=04h Bit5,4)= 1, 2 or 3
Address=22h, Data=10h (Default Data=26h)
Address=24h, Data=0Fh (Default Data=27h)
Address=28h, Data=06h (Default Data=23h)

POWER ON SEQUENCE



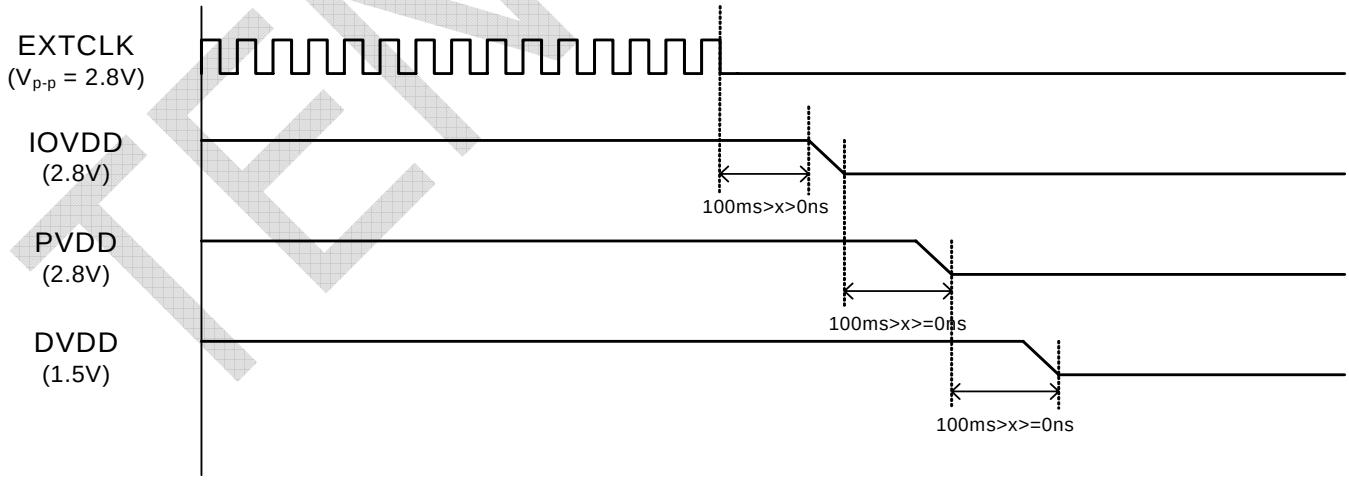
* ((VOUTPH + 3) - VRRPH) + 4
In default case: VOUTPH=35dec, VRRPH=38dec, ((35 + 3) - 38) + 4 = 4H

D_MASK=1

TCM8230MD cannot output pictures after power on immediately. You should be sent some I^2C commands after power on as below.

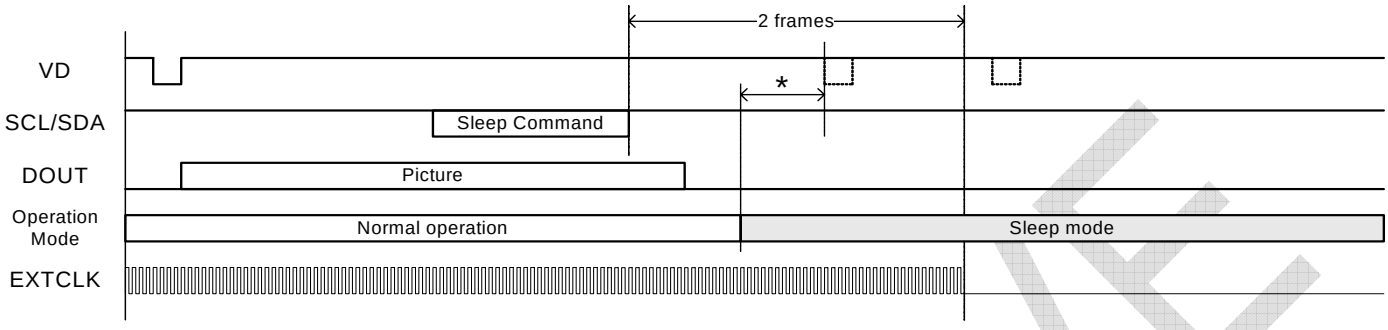
Address=03h, Data=00h (Default Data=80h)

POWER OFF SEQUENCE



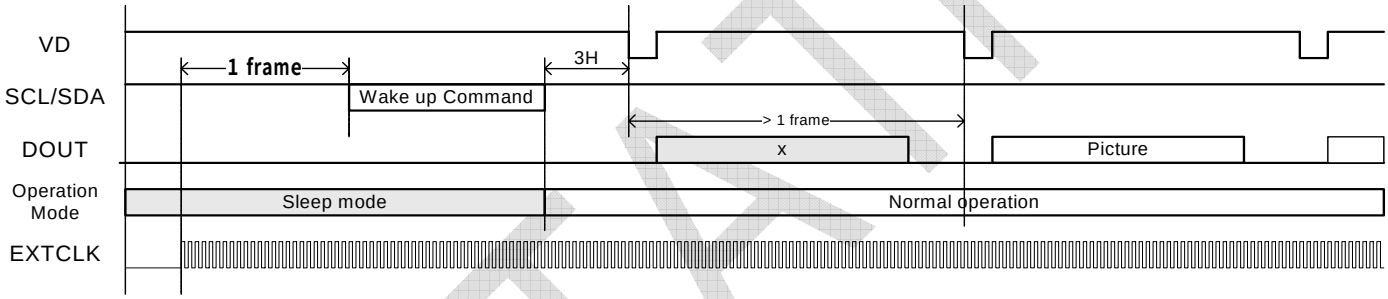
SLEEP MODE SEQUENCE

1. From normal operation to sleep mode



* ((VOUTPH + 3) - VRRPH) + 4
In default case: VOUTPH=35dec, VRRPH=38dec, ((35 + 3) - 38) + 4 = 4H

2. From sleep mode to normal operation



D_MASK=1

Some registers data, AWB calculated data and ALC calculated data are kept the last values during sleep mode.

MAXIMUM RATING

	RATING		UNITS
	1.5V	2.8V	
Power supply voltage	-0.3 to 3.0	-0.3 to 3.6	V
Storage tempature	-30 to 85		Degree C

RECOMMENDED OPERATING CONDITION

		MIN	TYP	MAX	UNITS
Power supply voltage	IOVDD, PVDD*	2.6	2.8	3.0	V
		2.3	2.5	2.7	
	DVDD	1.4	1.5	1.6	
Operational tempature		-20	-	60	Degree C

*If using 2.5V, must input setting command. (Default setting is 2.8V.)

ELECTRICAL CHARACTERISTICS

DC Characteristic (Ta=25 degree C, DVDD(=AVDD) =1.5V, PVDD= IOVDD =2.8V)

1. POWER

ITEM	CONDITION	MIN	TYP	MAX	UNITS
POWER	VGA(15fps) (Normal operation mode)	-	40	TBD	mA
	Sleep mode	-	-	TBD	uA

* Measurement condition : Machbeth chart (full)
*Peak current = 180mA

2. EXTCLK

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Rectangular shape	LOW level input voltage	$V_{IL;EXTCLK}$	-	-0.3	-	IOVDD*0.2	V	
	HIGH level input voltage	$V_{IH;EXTCLK}$	-	IOVDD*0.8	IOVDD	3.0	V	
	LOW level input current	$I_{IL;EXTCLK}$	V_{IN}=GND	-10	-	10	uA	
	HIGH level input current	$I_{IH;EXTCLK}$	V_{IN}=IOVDD	-10	-	10	uA	
	DUTY	-	-	45/55	50/50	55/45	%	*1

1) Duty referred to 50% level of input EXTCLK

3. SCL and SDA

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
SCL	LOW level input voltage	$V_{IL;SCL}$	0.0	-	0.4	V	
	HIGH level input voltage	$V_{IH;SCL}$	IOVDD*0.7	IOVDD	3.0	V	
SDA	LOW level input voltage	$V_{IL;SDA}$	0.0	-	0.4	V	
	HIGH level input voltage	$V_{IH;SDA}$	IOVDD*0.7	IOVDD	3.0	V	
	LOW level output voltage (IOL=4mA)	$V_{OL;SDA}$	0.0	-	0.4	V	

4. DOUT0 to DOUT7, DCLK, HD and VD

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
DOUT0 to DOUT7, DCLK, HD and VD	LOW level output voltage (IOL=2mA)	$V_{OL;DATA}$	0.0	-	0.4	V	
	HIGH level output voltage (IOH=-2mA)	$V_{OH;DATA}$	2.4	IOVDD	-	V	

5. RESET

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTES
LOW level input voltage	$V_{IL;RESET}$	-	-0.3	-	IOVDD*0.2	V	
HIGH level input voltage	$V_{IH;RESET}$	-	IOVDD*0.8	IOVDD	3.0	V	
LOW level input current	$I_{IL;RESET}$	V_{IN}=GND	-10	-	10	uA	
HIGH level input current	$I_{IH;RESET}$	V_{IN}=IOVDD	-10	-	10	uA	

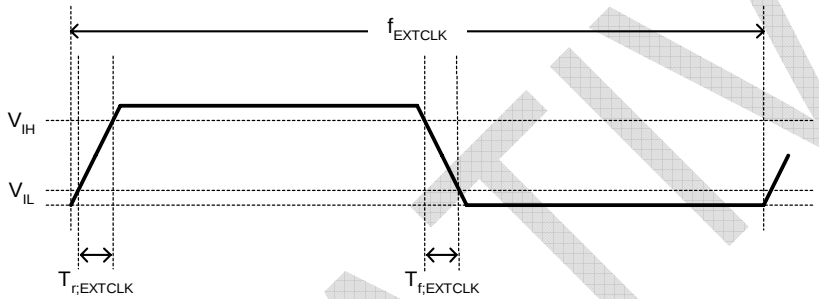
AC Characteristic (Ta=25 degree C, DVDD(=AVDD) =1.5V, PVDD= IOVDD =2.8V)

1. EXTCLK

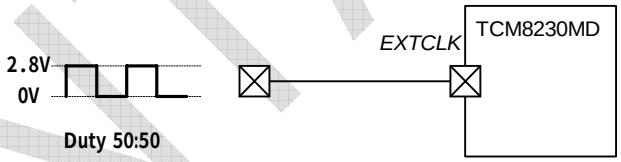
ITEM	SYMBOL	FPS	MIN	TYP	MAX	UNITS	NOTES
Clock frequency	f_{EXTCLK}	0	11.90	24.54	25.00	MHz	*1
		1			27.00		
Rise time	$t_{r;EXTCLK}$	-	-	-	5	ns	*2
Fall time	$t_{f;EXTCLK}$	-	-	-	5	ns	

1) FPS : Address=02h, Bit7

2) All values referred to V_{IHmin} and V_{ILmax} levels



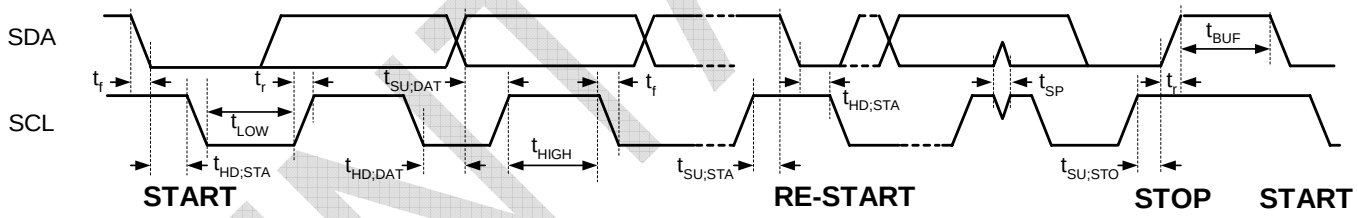
2. EXTCLK input circuit



3. SCL and SDA

ITEM		SYMBOL	MIN	MAX	UNITS	NOTES
SCL	Clock frequency	f_{SCL}	-	400	KHz	*1
	Low period	$t_{LOW;SCL}$	1.3	-	us	
	High period	$t_{HIGH;SCL}$	0.6	-	us	
	Rise time	$t_{r;SCL}$	-	300	ns	
	Fall time	$t_{f;SCL}$	-	300	ns	
SDA	Rise time	$t_{r;SDA}$	-	300	ns	
	Fall time	$t_{f;SDA}$	-	300	ns	
Hold time(repeated) START condition After this period, the first clock pulse is		$t_{HD;STA}$	0.6	-	us	
Setup time for a repeated START condition		$t_{SU;STA}$	0.6	-	us	
Data hold time		$t_{HD;DAT}$	0	-	ns	
Data setup time		$t_{SU;DAT}$	100	-	ns	
Setup time for STOP condition		$t_{SU;STO}$	0.6	-	us	
Width of spike pulse	Normal	t_{SP1}	0	50	ns	
	Wake-up from sleep mode	t_{SP2}	0	20	ns	

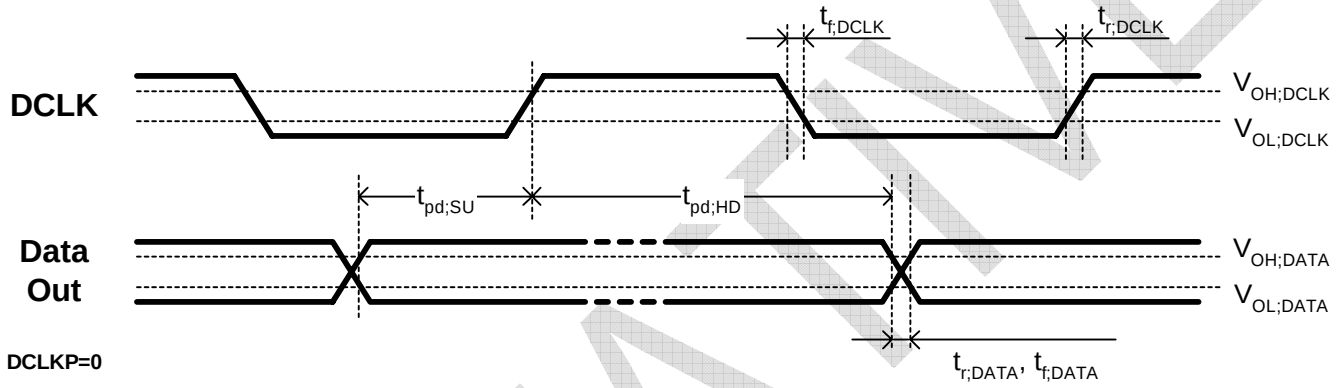
1) All values referred to V_{IHmin} and V_{ILmax} levels



4. DOUT0 to DOUT7, DCLK, HD and VD

ITEM		SYMBOL	MIN	MAX	UNITS	NOTES
DCLK	Rise time	$t_{r;DCLK}$	-	6	ns	*1
	Fall time	$t_{f;DCLK}$	-	6	ns	
DOUT0 to DOUT7, HD, and VD	Rise time	$t_{r;DATA}$	-	6	ns	
	Fall time	$t_{f;DATA}$	-	6	ns	
Setup time of data		$t_{pd;SU}$	10	-	ns	
Hold time of data		$t_{pd;HD}$	10	-	ns	

1) All values referred to V_{OHmin} and V_{OLmax} levels



CHARACTERISTICS OF LENS

ITEM		VALUE	UNITS
Optical format		1/6	inch
Field of view	Holizontal	57.4	degree
	Vertical	44.5	degree
	Diagonal	69.1	degree
F number		F2.8	-
TV distotion		-0.4	%
Focal length		TBD	mm
Focusing area		TBD	cm
Manual focusing		Not avairable	-
Structure		Double lens	-

Appendix 1: Module Drawing