

## **Product Specifications**

Customer	Standard
Description	2.0" TFT EPD Panel
Model Name	EG020AS012
Date	2013/07/15
Doc. No.	1P001-00
Revision	04

Customer Approval					
Date					
-	represents that the product specifications, ty in the specifications are accepted	testing			

Des	Design Engineering			
Approval Check Design				
<del>黄</del> 2013.7.15 富瑞	弊 2013.7.15 伊琳	集 2013.7.15 儀珍		

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## **Revision History**

Version	Date	Page (New)	Section	Description
Ver.01	2011/05/23	All	All	Approval specification first issued.
Ver.02	2012/02/24	15	9	Add module Label.
Ver.03	2012/06/20	All	All	Revise document format.
		12	1	Modify EPD drawing
		13	2.2	Add Note 3 at Reliability Test Items
15		15	3.2	Add current value(MAX) Add Note description
Ver.04	2013/07/15	17	5.1	Modify description in Terminal Pin Assignment
	, _,	19	5.2	Modify Reference circuit
		6.2.2	About refreshing of Test1 & Test2 had modified "1h storage" to "Refresh immediately", and to delete the PCS test.	
		28	0	Madify definition of labols
		29	9	Modify definition of labels

## **Glossary of Acronyms**

ctrophoretic Display (e-Paper Display)
)
D with TCon board
ning Controller
n Film Transistor
rocontroller Unit
xible Printed Circuit
nt Plane Laminate
ial Peripheral Interface
p on Glass
nt Contrast Signal
vasive Displays Incorporated

## **1** General Description

### 1.1 Overview

This is a 2.0" a-Si, active matrix TFT, Electronic Paper Display (EPD) panel. The panel has such high resolution (111 dpi) that it is able to easily display fine patterns. Due to its bi-stable nature, the EPD panel requires very little power to update and needs no power to maintain an image.

### 1.2 Features

- a-Si TFT active matrix Electronic Paper Display(EPD)
- Resolution: 200 x 96
- Ultra low power consumption
- Super Wide Viewing Angle near 180°
- Extra thin & light
- SPI interface
- RoHS compliant

### 1.3 Applications

- Electronic shelf label (ESL)
- Reusable container
- Badge

## **1.4 General Specifications**

#### Table 1-1 General Specification

Item	Specification	Unit	Note
Outline Dimension	57.0(H) x 28.8(V) x 1.0(T)		(1)
Active Area	45.800(H) x 21.984(V)	mm	
Driver Element	a-Si TFT active matrix	-	
FPL	V110	-	
Pixel Number	200 x 96	pixel	
Pixel Pitch	0.229 x 0.229 (111dpi)	mm	
Pixel Arrangement	Vertical stripe	-	
Display Colors	Black/White	-	
Surface Treatment	Anti-Glare	-	

Note (1): Not including the FPC.

## **1.5 Mechanical Specifications**

### Table 1-2 Mechanical Specification

Item		Min.	Тур.	Max.	Unit	Note
Glass Size	Horizontal(H)	56.7	57.0	57.3	mm	
	Vertical(V)	28.5	28.8	29.1	mm	
	Thickness(T)	0.8	1.0	1.2	mm	(1)
Weight			3.7	4.5	g	

Note (1): Not including the Masking Film.

### Table 1-3 FPC Specification

Item	Pin numbers	Pitch (mm)	Connector	Note
Golden Finger	40	0.5	STARCONN 089H40 or Compatible	

### Figure 1-1 EPD Drawing



General tolerance: ±0.3mm

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## 2 Absolute Maximum Ratings

### 2.1 Absolute Ratings of Environment

### Table 2-1 Absolute Ratings of Environment

Itom	Cumbol	Value		Unit	Noto
Item	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T <sub>ST</sub>	-20	+60	٥C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	+50	٥C	(1), (2)

Note (1):

- (a) 90 %RH Max. (Ta  $\leq$  40 °C), where Ta is ambient temperature.
- (b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).
- (c) No condensation.
- Note (2): The temperature of panel display surface area should be 0 °C Min. and 50 °C Max. Refresh time depends on operation temperature.

### Figure 2-1 Operating Range of Relative Humidity and Temperature





## 2.2 Reliability Test Item

### Table 2-2 Reliability Test I tems

Item	Test Condition	Remark
High Temperature Operation	50 ℃ for 240h	(1)(2)
Low Temperature Operation	0 °C for 240h	(1) (2)
High Temperature/Humidity Operation	40 $^\circ C$ / 90 %RH for 168h	(1) (2)
High Temperature Storage	60 ℃ for 240h	(1) (2)(3)
Low Temperature Storage	-20 ℃ for 240h	(1) (2) (3)
High Temperature/Humidity Storage	50 $^\circ C$ / 80 %RH for 168h	(1) (2) (3)
Thermal Cycles ( Non-operation )	1 Cycle:-20°C/30min → 60°C/30min, for 100 Cycles	(1) (2) (3)
Package Drop Test	Drop from 97cm. ( ISTA ) 1 corner, 3 edges, 6 sides. One drop for each.	(1) (2) (3)
Package Random Vibration Test	1.15Grms, 1Hz ~ 200Hz. ( ISTA )	(1) (2) (3)

Note (1): End of test, function, mechanical, and optical shall be satisfied.

- Note (2): The test result and judgment are based on PDI's 1bit driving waveform, driving fixture and driving system.
- Note (3): Test with white pattern

## **3** Electrical Characteristics

## 3.1 Absolute Maximum Ratings of Panel

### Table 3-1 Absolute Maximum Ratings of Panel

Darameter	Cumbol	Value		Unit	Neto
Parameter Syn	Symbol	Min	Max	Unit	Note
Digital Power	$V_{\text{DD}}$	-0.3	5.0	V	
Analog Power	V <sub>cc</sub>	-0.3	5.0	V	
Ground	V <sub>SS</sub>		-	-	Connect $V_{ss}$ to Ground

Ta = 25 ± 2 °C

## 3.2 Recommended Operation Conditions of Panel

### Table 3-2 Recommended Operation Conditions of Panel

Darameter		Symbol		Value		Unit	Noto
Pala	Parameter	Symbol	Min	Тур	Max	Unit	Note
Digita	l Power	$V_{\text{DD}}$	2.7	3.0	3.3	V	
Analo	g Power	$V_{CC}$	2.7	3.0	3.3	V	
Input	High	$V_{\mathrm{IH}}$	$0.8V_{DD}$	-	$V_{DD}$	V	/CS, ID, SCLK,
Voltage Low	V <sub>IL</sub>	$V_{SS}$	-	$0.2V_{DD}$	V	SI, /RESET	
Output	High	V <sub>OH</sub>	$0.8V_{DD}$	-	V <sub>DD</sub>	V	I <sub>OH</sub> =0.5mA, SO, BUSY
Voltage	Low	V <sub>OL</sub>	$V_{SS}$	-	$0.2V_{DD}$	V	I <sub>OL</sub> =-0.5mA, SO, BUSY
Input	High	$I_{\mathrm{IH}}$	-	-	1.0	uA	
Leakage Current	Low	$\mathbf{I}_{IL}$	-	-	-1.0	uA	

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Input Current	$I_{DD} + I_{CC}$	-	4	8	mA	(1),(2),(3)
DC/DC Inrush Current	$\mathbf{I}_{PEAK}$	-	40	100	mA	(1),(2),(3)
						Ta = 25 ± 2 °C

Note (1):





These currents are tested with PDI test jig.

Note (2):

 $V_{DD}=V_{CC}=3.0V$ 

### Figure 3-2 Image Update Current Profile



The "Time of DC/DC ON" which contains the some current peak of  $V_{GH}/V_{DH}/V_{GL}/V_{DL}/V_{COM}.$ 

Note (3):





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## 4 Application Circuit Block Diagram

### Figure 4-1 Application Circuit Block Diagram



## 5 Terminal Pin Assignment & Reference Circuit

## 5.1 Terminal Pin Assignment

#### Table 5-1 Terminal Pin Assignment

No.	Signal	Туре	Connected to	Function
1	/CS	I	Tcon	Chip Select. Low enable
2	BUSY	0	Tcon	When BUSY = HIGH, EPD stays in busy state that EPD ignores any input data from SPI
3	ID	Ι	Ground	Connect ID to ground
4	SCLK	Ι	Tcon	Clock for SPI
5	SI	I	Tcon	Serial input from Timing Controller to EPD
6	SO	О	Tcon	Serial output from EPD to Timing Controller
7	/RESET	Ι	Tcon	Reset signal. Low enable
8	ADC_IN	-	-	Not connected
9	V <sub>CL</sub>	С	Capacitor	
10	C42P	С	Charge-Pump	
11	C42M	С	Capacitor	
12	C41P	С	Charge-Pump	
13	C41M	С	Capacitor	
14	C31M	С	Charge-Pump	
15	C31P	С	Capacitor	
16	C21M	С	Charge-Pump	
17	C21P	С	Capacitor	
18	C16M	С	Charge-Pump	
19	C16P	С	Capacitor	
20	C15M	С	Charge-Pump	
21	C15P	С	Capacitor	

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22C14MCCharge-Pump CapacitorImage: Capacitor23C14PCCharge-Pump CapacitorImage: Capacitor24C13MCCharge-Pump CapacitorImage: Capacitor25C13PCCharge-Pump CapacitorImage: Capacitor26C12MCCharge-Pump CapacitorImage: Capacitor27C12PCCharge-Pump CapacitorImage: Capacitor28C11MCCharge-Pump CapacitorImage: Capacitor30V_{COM_DRIVERRCResistor & CapacitorThe signal duty cycle can drive VCOM voltage from source driver IC31VcccPVcccPower supply for analog part of source driver32VbbPVbbPower supply for digital part of source driver33VssPGround34VGHCCapacitor35VGLCCapacitor36VDHCCapacitor37VbLCCapacitor38BORDERI-40Vcom_PAMELCCapacitor					
23C14PCC24C13MCCharge-Pump Capacitor	22	C14M	С		
25C13PCCharge-Pump Capacitor26C12MCCharge-Pump Capacitor	23	C14P	С	Capacitor	
23CLISPC26C12MCCharge-Pump Capacitor	24	C13M	С	Charge-Pump	
27C12PCCharge-Pump Capacitor28C11MCCharge-Pump Capacitor	25	C13P	С	Capacitor	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	26	C12M	С	Charge-Pump	
29C11PCCharge-Pump Capacitor30V_{COM_DRIVER}RCResistor & CapacitorThe signal duty cycle can drive VCOM voltage from source driver IC31V_{CC}PV_{CC}Power supply for analog part of source driver32V_{DD}PV_{DD}Power supply for digital part of source driver33V_{SS}PGround34V_{GH}CCapacitor35V_{GL}CCapacitor36V_{DH}CCapacitor37V_{DL}CCapacitor38BORDERI-Connect to V_{DL} via control circuit for white frame border39V_{ST}PV_{COM_PANEL	27	C12P	С	Capacitor	
25       CTIP       C       Resistor       Resistor & Capacitor       The signal duty cycle can drive VCOM voltage from source driver IC         30       V <sub>COM_DRIVER</sub> RC       Resistor & Capacitor       The signal duty cycle can drive VCOM voltage from source driver IC         31       V <sub>CC</sub> P       V <sub>CC</sub> Power supply for analog part of source driver         32       V <sub>DD</sub> P       V <sub>DD</sub> Power supply for digital part of source driver         33       V <sub>SS</sub> P       Ground       Ground       Ground         34       V <sub>GH</sub> C       Capacitor       Capacitor         36       V <sub>DH</sub> C       Capacitor       Capacitor         37       V <sub>DL</sub> C       Capacitor       Connect to V <sub>DL</sub> via control circuit for white frame border         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border	28	C11M	С	Charge-Pump	
30       V <sub>COM_DRIVER</sub> RC       Resistor & Capacitor       voltage from source driver IC         31       V <sub>CC</sub> P       V <sub>CC</sub> Power supply for analog part of source driver         32       V <sub>DD</sub> P       V <sub>DD</sub> Power supply for digital part of source driver         33       V <sub>SS</sub> P       Ground       Power supply for digital part of source driver         34       V <sub>GH</sub> C       Capacitor       Power supply for digital part of source driver         35       V <sub>GL</sub> C       Capacitor       Power supply for digital part of source driver         36       V <sub>DH</sub> C       Capacitor       Power supply for digital part of source driver         37       V <sub>DL</sub> C       Capacitor       Power supply for digital part of source driver         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border         39       V <sub>ST</sub> P       V <sub>COM_PANEL</sub> Power supply for digital part of source driver	29	C11P	С	Capacitor	
31       V <sub>CC</sub> P       V <sub>CC</sub> source driver         32       V <sub>DD</sub> P       V <sub>DD</sub> Power supply for digital part of source driver         33       V <sub>SS</sub> P       Ground       Ground         34       V <sub>GH</sub> C       Capacitor         35       V <sub>GL</sub> C       Capacitor         36       V <sub>DH</sub> C       Capacitor         37       V <sub>DL</sub> C       Capacitor         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border         39       V <sub>ST</sub> P       V <sub>COM_PANEL</sub>	30	V <sub>COM_DRIVER</sub>	RC	Resistor & Capacitor	
32       V <sub>DD</sub> P       V <sub>DD</sub> source driver         33       V <sub>SS</sub> P       Ground       34         34       V <sub>GH</sub> C       Capacitor         35       V <sub>GL</sub> C       Capacitor         36       V <sub>DH</sub> C       Capacitor         37       V <sub>DL</sub> C       Capacitor         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border         39       V <sub>ST</sub> P       V <sub>COM_PANEL</sub>	31	V <sub>cc</sub>	Р	V <sub>cc</sub>	
34       V <sub>GH</sub> C       Capacitor         35       V <sub>GL</sub> C       Capacitor         36       V <sub>DH</sub> C       Capacitor         37       V <sub>DL</sub> C       Capacitor         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border         39       V <sub>ST</sub> P       V <sub>COM_PANEL</sub> V	32	V <sub>DD</sub>	Р	V <sub>DD</sub>	
35       V <sub>GL</sub> C       Capacitor         36       V <sub>DH</sub> C       Capacitor         37       V <sub>DL</sub> C       Capacitor         38       BORDER       I       -       Connect to V <sub>DL</sub> via control circuit for white frame border         39       V <sub>ST</sub> P       V <sub>COM_PANEL</sub> V	33	V <sub>SS</sub>	Р	Ground	
36     V <sub>DH</sub> C     Capacitor       37     V <sub>DL</sub> C     Capacitor       38     BORDER     I     -     Connect to V <sub>DL</sub> via control circuit for white frame border       39     V <sub>ST</sub> P     V <sub>COM_PANEL</sub> -	34	$V_{GH}$	С	Capacitor	
37     V <sub>DL</sub> C     Capacitor       38     BORDER     I     -     Connect to V <sub>DL</sub> via control circuit for white frame border       39     V <sub>ST</sub> P     V <sub>COM_PANEL</sub> I	35	V <sub>GL</sub>	С	Capacitor	
38     BORDER     I     -     Connect to V <sub>DL</sub> via control circuit for white frame border       39     V <sub>ST</sub> P     V <sub>COM_PANEL</sub>	36	V <sub>DH</sub>	С	Capacitor	
36     DORDER     1     -     white frame border       39     V <sub>ST</sub> P     V <sub>COM_PANEL</sub> -	37	V <sub>DL</sub>	С	Capacitor	
	38	BORDER	I	-	
40     V <sub>COM_PANEL</sub> C     Capacitor     V <sub>COM</sub> to panel	39	V <sub>ST</sub>	Р	V <sub>COM_PANEL</sub>	
	40	V <sub>COM_PANEL</sub>	С	Capacitor	V <sub>COM</sub> to panel

Note:

Type:	I:	Input
iype.	1.	Input

- O: Output
- C: Capacitor
- RC: Resistor and Capacitor
- P: Power

## 5.2 Reference Circuit

### Figure 5-1 EPD Reference Circuit





## **6** Optical Characteristics

### 6.1 Test Conditions

### Table 6-1 Optical Test Conditions

Item	Symbol	Value	Unit
Ambient Temperature	Та	25±2	٥C
Ambient Humidity	На	50±10	%RH
Supply Voltage	V <sub>CC</sub> & V <sub>DD</sub>	3.0	V

### 6.2 Optical Specifications

### 6.2.1 Optical

#### Table 6-2 Optical Measurement with D65 light source

Theres	Cumahal	Rating				Nata
Item	Symbol	Min.	Тур.	Max.	Unit	Note
Contract ratio	CD	<b>E</b> .1	7.1			$\theta x = \theta y = 0$
Contrast ratio	CR	5:1	7:1	-	-	(1),(2),(3),(4)
Refresh time	Tr	-	2	-	sec	(3)
White Chromaticity	Wx		0.313		-	$\theta x = \theta y = 0$
		-		-		(1),(4)
	Wy	-	0.338	-		
Reflectance	R%	25	32	-	%	(1),(4)



Note (1): Panel is driven by PDI waveform without masking film and optical measurement by CM-700D with D65 light source and SCE mode.

#### Figure 6-1 Optical measurement





Note (2): Definition of Viewing Angle ( $\theta x$ ,  $\theta y$ ):

#### Figure 6-2 Definition of Viewing Angle to Measure Contrast Ratio



- Note (3): Refresh time is the time that e-paper particles move not including the power on and off time. The refresh time is measured at 25°C. The refresh time and contrast ratio varies due to different films, display performance requirements, and ambient temperatures.
- Note (4): Contrast ratio (C.R.): The Contrast ratio is calculated by the following expression. C.R. =(R% White) / (R% Black). Reflectance is measured at 120 seconds after refresh.



## 6.2.2 Ghosting

Below are two test methods to verify that ghosting within an acceptable range. Test 1 and Test 2 use measured data to calculate Delta E which is a single number representing the distance between two colors in a 3 dimensional color space. Test 1 and test 2 are performed at 25°C.

• Test 1: White to Black Ghosting



Test 2: Black to White Ghosting



The formula is used to calculate Test1 and Test2. For example of Test 2:  $\Delta E^*ab = [(L_B - L_{B'})^2 + (a_B - a_{B'})^2 + (b_B - b_{B'})^2]^{1/2}$ 

Table 6-3 Measurement of Ghosting

Itom	Rating				
Item	Min.	Тур.	Max.		
Test 1 ∆E*ab	-	-	2		
Test 2 ∆E*ab	-	-	2		

Note: Panel is driven by PDI waveform without masking film and optical measurement by CM-700D with D65 light source and SCE mode.

## 7 Packing





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### 459(pcs) x 40(BOX)=18,360pcs

	2″ EPD BOX	
N.W. :	1.47Kg	
G.W. :	4.83Kg	

## Sea / Land / Air Transportation



## 8 Precautions

- (1) The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel during assembly.
- (2) It is recommended to assemble or install EPD panels in a clean working area. Dust and oil may cause electrical shorts or degrade the protection sheet film.
- (3) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (4) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (5) Please support the bezel with your finger while connecting the interface cable such as the FPC.
- (6) Do not stack the EPD panels / Modules.
- (7) Do not press the FPC on the glass edge or Pull FPC up / down to 90°.
- (8) Do not touch the FPC lead connector.
- (9) Wear a Wrist Strap (Grounding connect) when handling and during assembly. Semiconductor devices are included in the EPD Panel / Module and they should be handled with care to prevent any electrostatic discharge (ESD). (An Ion Fan may be needed in assembly operation to reduce ESD risk.)
- (10) Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching.
- (11) Do not disassemble or reassemble the EPD panel.
- (12) Use a soft dry cloth without chemicals for cleaning. The surface of the protection sheet film is very soft and easily scratched.
- (13) Be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (14) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. It is highly recommended to store the EPD panel in a dark place without condensation, a temperature range of 15°C to 35°C, and humidity from 30%RH to 60%RH.
- (15) The ink used for marking the Panel ID number is erased easily by solvent. Please avoid using solvent to clean the EPD panel.
- (16) The EPD is vacuum packed.
- (17) Before approved by PDI and customer, products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
- (18) PDI makes every attempt to ensure that its products are of high quality and reliability. However, contact PDI sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

- (19) Design your application so that the product is used within the ranges guaranteed by PDI particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. PDI bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail safes, so that the equipment incorporating PDI product does not cause bodily injury, fire or other consequential damage due to operation of the PDI product.
- (20) This product is not designed to be radiation resistant.

## 9 Definition of Labels

Figure 9-1 Model Labels



## Figure 9-2 Definition of Model Labels





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Bar Code=Model Name.+Pallet Serial No.+Q'TY.(22 Digits)

## Pallet Label

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