

T8000

LCD Controller Technical Manual

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Table of Content

1. Introduction	3
2. Features Highlight	3
3. IC Layout	4
3.1 Pads Layout Diagram.....	4
3.2 Pads Coordinates.....	5
3.3 Pads Descriptions	6
4. Hardware Configuration on RESET	8
5. Memory Mappings	9
5.1 Memory Configuration.....	9
5.2 Memory Mapped Peripheral Configuration Registers.....	9
6. Function Specifications	10
6.1 Function Block	10
6.2 Command Interpreter	10
6.3 Command Packet Format	11
6.4 Opcode Description.....	11
6.5 Opcode Descriptions.....	12
6.6 RS232 Serial Host Communication Packet Format.....	13
7. LCD Controller	14
7.1 LCD Controller Structure.....	14
7.2 Display Data Format	15
7.3 Sprite / Overlay Controller.....	16
7.4 2D Hardware Acceleration Controller.....	17
7.5 Memory Controller.....	17
7.6 Host Hub	18
7.7 GPIO	18
7.8 OSC and PLL.....	18
7.9 Registers Settings	19
8. Electrical Characteristics	23
8.1 Absolute Maximum Ratings	23
8.2 Recommended Operating Conditions	23
8.3 DC Characteristics	23
8.4 AC Characteristics	24
8.5 Power Save Mode.....	32
9. Revision Note.....	33

1. Introduction

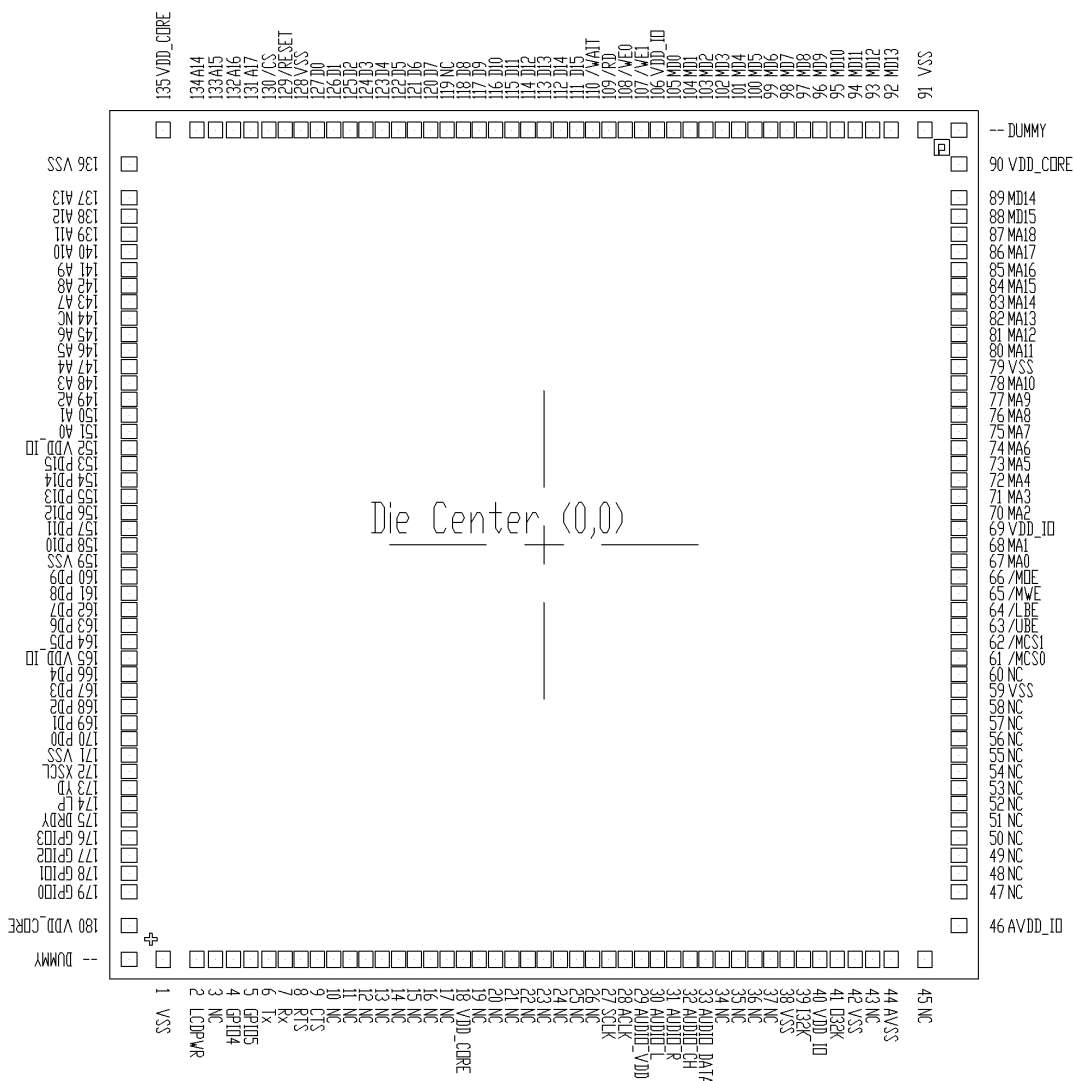
This Technical manual describes the features, options and connections of the T8000 Graphics Controller. T8000 is a high performance graphics controller supporting mono LCD display to TFT color LCD display. T8000 embed with 2D geometry drawing engine as well as font handling engine data (ASCII, Big5, GB2312).

2. Features Highlight

- Power Supply
 - 3.3V supply voltage
 - 3.3V logic I/O (tolerate to 5V logic input from host)
 - 2.5V core voltage
- Display Memory
 - Built in display SRAM 56k bytes SRAM
 - Support external display SRAM up to 128k byte (cascaded to the embedded SRAM)
 - Support external font ROM (up to 1M byte)
- Display Support
 - Up to 64k color, TFT LCD display
 - Up to 4096 color, CSTN LCD display (4bit or 8bit interface)
 - Up to 16 gray, Mono passive LCD display (4bit or 8bit interface)
- Host Interface
 - 8bit data, 1bit address
 - 8bit data, 16bit address
 - 16bit data, 16bit address
 - UART
- 2D Drawing Engine
 - Line Draw
 - Circuit Draw
 - Circuit Draw with solid fill
 - Box Draw
 - Box Draw with solid fill
- Font Draw Engine
 - Support 8bit (eg. ASCII) char coding & 16bit char coding (eg GB2312, BIG5)
 - Support 8x8, 8x16 and 16x16 font size with color expansion
- Display Features
 - Virtual display with pixel panning in all color depths
 - Hardware Sprite / overlay
- Others
 - 5 GPIOs
 - Built-in PLL with standard 32.768kHz Crystal as clock source

3. IC Layout

3.1 Pads Layout Diagram





3.2 Pads Coordinates

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		x	y			x	y			x	y
1	VSS	-2470	-2690	61	/MCS0	2690	-735	121	D6	-840	2690
2	LCDPWR	-2250	-2690	62	/MCS1	2690	-630	122	D5	-945	2690
3	NC	-2130	-2690	63	/UBE	2690	-525	123	D4	-1050	2690
4	GPIO4	-2015	-2690	64	/LBE	2690	-420	124	D3	-1155	2690
5	GPIO5	-1900	-2690	65	/MWE	2690	-315	125	D2	-1260	2690
6	TX	-1785	-2690	66	/MOE	2690	-210	126	D1	-1365	2690
7	RX	-1680	-2690	67	MA0	2690	-105	127	D0	-1470	2690
8	RTS	-1575	-2690	68	MA1	2690	0	128	VSS	-1575	2690
9	CTS	-1470	-2690	69	VDD_IO	2690	105	129	/RESET	-1680	2690
10	NC	-1365	-2690	70	MA2	2690	210	130	/CS	-1785	2690
11	NC	-1260	-2690	71	MA3	2690	315	131	A17	-1900	2690
12	NC	-1155	-2690	72	MA4	2690	420	132	A16	-2015	2690
13	NC	-1050	-2690	73	MA5	2690	525	133	A15	-2130	2690
14	NC	-945	-2690	74	MA6	2690	630	134	A14	-2250	2690
15	NC	-840	-2690	75	MA7	2690	735	135	VDD_CORE	-2470	2690
16	NC	-735	-2690	76	MA8	2690	840	136	VSS	-2690	2470
17	NC	-630	-2690	77	MA9	2690	945	137	A13	-2690	2250
18	VDD_CORE	-525	-2690	78	MA10	2690	1050	138	A12	-2690	2130
19	NC	-420	-2690	79	VSS	2690	1155	139	A11	-2690	2015
20	NC	-315	-2690	80	MA11	2690	1260	140	A10	-2690	1900
21	NC	-210	-2690	81	MA12	2690	1365	141	A9	-2690	1785
22	NC	-105	-2690	82	MA13	2690	1470	142	A8	-2690	1680
23	NC	0	-2690	83	MA14	2690	1575	143	A7	-2690	1575
24	NC	105	-2690	84	MA15	2690	1680	144	NC	-2690	1470
25	NC	210	-2690	85	MA16	2690	1785	145	A6	-2690	1365
26	NC	315	-2690	86	MA17	2690	1900	146	A5	-2690	1260
27	SCLK	420	-2690	87	MA18	2690	2015	147	A4	-2690	1155
28	ACLK	525	-2690	88	MD15	2690	2130	148	A3	-2690	1050
29	AUDIO_VDD	630	-2690	89	MD14	2690	2250	149	A2	-2690	945
30	AUDIO_L	735	-2690	90	VDD_CORE	2690	2470	150	A1	-2690	840
31	AUDIO_R	840	-2690	91	VSS	2470	2690	151	A0	-2690	735
32	AUDIO_CH	945	-2690	92	MD13	2250	2690	152	VDD_IO	-2690	630
33	AUDIO_DATA	1050	-2690	93	MD12	2130	2690	153	PD15	-2690	525
34	NC	1155	-2690	94	MD11	2015	2690	154	PD14	-2690	420
35	NC	1260	-2690	95	MD10	1900	2690	155	PD13	-2690	315
36	NC	1365	-2690	96	MD9	1785	2690	156	PD12	-2690	210
37	NC	1470	-2690	97	MD8	1680	2690	157	PD11	-2690	105
38	VSS	1575	-2690	98	MD7	1575	2690	158	PD10	-2690	0
39	I32K	1680	-2690	99	MD6	1470	2690	159	VSS	-2690	-105
40	VDD_IO	1785	-2690	100	MD5	1365	2690	160	PD9	-2690	-210
41	O32K	1900	-2690	101	MD4	1260	2690	161	PD8	-2690	-315
42	VSS	2015	-2690	102	MD3	1155	2690	162	PD7	-2690	-420
43	NC	2130	-2690	103	MD2	1050	2690	163	PD6	-2690	-525
44	AVSS	2250	-2690	104	MD1	945	2690	164	PD5	-2690	-630
45	NC	2470	-2690	105	MD0	840	2690	165	VDD_IO	-2690	-735
46	AVDD_IO	2690	-2470	106	VDD_IO	735	2690	166	PD4	-2690	-840
47	NC	2690	-2250	107	/WE1	630	2690	167	PD3	-2690	-945
48	NC	2690	-2130	108	/WE0	525	2690	168	PD2	-2690	-1050
49	NC	2690	-2015	109	/RD	420	2690	169	PD1	-2690	-1155
50	NC	2690	-1900	110	/WAIT	315	2690	170	PD0	-2690	-1260
51	NC	2690	-1785	111	D15	210	2690	171	VSS	-2690	-1365
52	NC	2690	-1680	112	D14	105	2690	172	XSCL	-2690	-1470
53	NC	2690	-1575	113	D13	0	2690	173	YD	-2690	-1575
54	NC	2690	-1470	114	D12	-105	2690	174	LP	-2690	-1680
55	NC	2690	-1365	115	D11	-210	2690	175	DRDY	-2690	-1785
56	NC	2690	-1260	116	D10	-315	2690	176	GPIO3	-2690	-1900
57	NC	2690	-1155	117	D9	-420	2690	177	GPIO2	-2690	-2015
58	NC	2690	-1050	118	D8	-525	2690	178	GPIO1	-2690	-2130
59	VSS	2690	-945	119	NC	-630	2690	179	GPIO0	-2690	-2250
60	NC	2690	-840	120	D7	-735	2690	180	VDD_CORE	-2690	-2470

3.3 Pads Descriptions

Power

Pad No.	Pad Name	Pad Type	Descriptions
1,38,42,59,79,91,128,136,159,171	VSS	POWER	Power Supply Ground (0V)
18,90,135,180	VDD_CORE	POWER	Positive Power Supply for Core (2.5V)
29	AUDIO_VDD	POWER	Positive Power Supply for Audio (3.3V)
40,69,106,152,165	VDD_IO	POWER	Positive Power Supply for IO (3.3V)
44	AVSS	POWER	Power Supply Ground for Analog (0V)
46	AVDD_IO	POWER	Positive Power Supply for Analog (3.3V)

Host Interface

Pad No.	Pad Name	Pad Type	Descriptions
107	/WE1	INPUT	Write signal strobe for high byte input
108	/WE0	INPUT	Write signal strobe for low byte input
109	/RD	INPUT	Read signal input, active low
110	/WAIT	OUTPUT	Wait signal, active low
111	D15	IO	High byte data for 16-bit interface
:	:		
118	D8		
120	D7	IO	8-bit data, for 8bit interface or Low byte data for 16-bit interface
:	:		
127	D0		
129	/RESET	INPUT	Hardware Reset, active low
130	/CS	INPUT	Chip select, active low
131	A17	INPUT	18-bit Host Address Input A0 ~ A17
:	:		
134	A14		
137	A13		
:	:		
143	A7		
145	A6		
:	:		
151	A0		

Note: Host interface could tolerate to 5V input.

LCD Interface

Pad No.	Pad Name	Pad Type	Descriptions
2	LCDPWR	OUTPUT	LCD Power Signal (/DISPLAYOFF or DISPLAYON)
153	PD15	OUTPUT	PD0~PD3, data for 4-bit STN Panel PD0~PD7, data for 8-bit STN or TFT Panel PD0~PD16, data for 16-bit TFT Panel
:	:		
158	PD10		
160	PD9		
:	:		
164	PD5		
166	PD4		
:	:		
170	PD0		
172	XSCL	OUTPUT	Pixel Shift Clock
173	YD	OUTPUT	Frame Start Signal for Vertical Sync
174	LP	OUTPUT	Line Pulse for Horizontal Sync
175	DRDY	OUTPUT	Data Ready Signal for TFT Panel or WF (M) Signal for STN panel

**External Memory Interface**

Pad No.	Pad Name	Pad Type	Descriptions
61	/MCS0	OUTPUT	External Memory Chip Select for SRAM
62	/MCS1	OUTPUT	External Memory Chip Select for ROM
63	/UBE	OUTPUT	External Memory Upper Byte Enable
64	/LBE	OUTPUT	External Memory Lower Byte Enable
65	/MWE	OUTPUT	External Memory Write Signal, Active Low
66	/MOE	OUTPUT	External Memory Output Signal, Active Low
67	MA0	OUTPUT	External Memory 18-bit Address BUS
68	MA1		
70	MA2		
:	:		
78	MA10		
80	MA11		
:	:		
87	MA18		
88	MD15	IO	External Memory 16-bit Data BUS
89	MD14		
92	MD13		
:	:		
105	MD0		

Audio Interface

Pad No.	Pad Name	Pad Type	Descriptions
27	SCLK	INPUT	Audio Shift Clock
30	AUDIO_L	OUTPUT	Audio Left Channel
31	AUDIO_R	OUTPUT	Audio Right Channel
32	AUDIO_CH	INPUT	IIS channel L/R
33	AUDIO_DATA	INPUT	IIS PCM Data

Clock and Others

Pad No.	Pad Name	Pad Type	Descriptions
4	GPIO4	IO	General purpose Input Output
5	GPIO5		
176	GPIO3		
:	:		
179	GPIO0		
28	ACLK	INPUT	Audio Master Clock Input
39	I32K	INPUT	Crystal Oscillator Input
41	O32K	OUTPUT	Crystal Oscillator Output
3,10-17,19-26, 34-37,43,45, 47-58,60,119,144	NC	-	No connection

4. Hardware Configuration on RESET

During hardware reset, value from memory data line, MD0~MD15, will be latched into an internal register for automatic system configurations. Except MD7, MD6 & MD0, modifying corresponding registers by the host could overwrite these settings.

All of the memory data lines are internal pull-down. (i.e. default is "0")

Pull-up the data line with a 10k resistor could provide a "1" for the RESET configuration.

The followings are the configuration table:

	Data Line										Descriptions
	MD15	MD12	MD11	MD10	MD9	MD8	MD7	MD6	MD5	MD4	
Config Group Panel Resolution	0000	-	-	-	-	-	-	-	-	-	User-defined
	0001	-	-	-	-	-	-	-	-	-	128x160
	0010	-	-	-	-	-	-	-	-	-	160x160
	0011	-	-	-	-	-	-	-	-	-	176x160
	0100	-	-	-	-	-	-	-	-	-	176x208
	0101	-	-	-	-	-	-	-	-	-	240x160
	0110	-	-	-	-	-	-	-	-	-	176x240
	0111	-	-	-	-	-	-	-	-	-	320x200
	1000	-	-	-	-	-	-	-	-	-	320x240
	1001	-	-	-	-	-	-	-	-	-	320x320 (mono STN only)
	1010	-	-	-	-	-	-	-	-	-	640x200 (mono STN only)
	1011	-	-	-	-	-	-	-	-	-	640x240 (mono STN only)
	1100	-	-	-	-	-	-	-	-	-	480x320 (mono STN only)
	1101	-	-	-	-	-	-	-	-	-	N/A
	1110	-	-	-	-	-	-	-	-	-	N/A
	1111	-	-	-	-	-	-	-	-	-	N/A
LCD I/F bus	-	0	-	-	-	-	-	-	-	-	4-bit I/F (using PD0~PD3)
	-	1	-	-	-	-	-	-	-	-	8-bit I/F (using PD0~PD7)
Panel and Color Depth	-	-	0	00	-	-	-	-	-	-	1bit-per-pixel (mono LCD panel)
	-	-	0	01	-	-	-	-	-	-	2bit-per-pixel (mono LCD panel)
	-	-	0	10	-	-	-	-	-	-	4bit-per-pixel (mono LCD panel)
	-	-	0	11	-	-	-	-	-	-	Reserved
	-	-	1	00	-	-	-	-	-	-	16bit-per-pixel, 5R-6G-5B (TFT LCD panel)
	-	-	1	01	-	-	-	-	-	-	12bit-per-pixel, 4R-4G-4B (CSTN LCD panel)
	-	-	1	10	-	-	-	-	-	-	Reserved
	-	-	1	11	-	-	-	-	-	-	Reserved
Host I/F	-	-	-	-	-	-	00	-	-	-	8bit generic (SRAM type) with WAIT signal
	-	-	-	-	-	-	01	-	-	-	16bit generic (big Endian SRAM type) with WAIT signal
	-	-	-	-	-	-	10	-	-	-	UART
	-	-	-	-	-	-	-	-	-	-	-
External Memory I/F	-	-	-	-	-	-	-	-	000	-	Ext SRAM : nil, Ext ROM : nil
	-	-	-	-	-	-	-	-	001	-	Ext SRAM : 8 x 64k, Ext ROM : nil
	-	-	-	-	-	-	-	-	010	-	Ext SRAM : 8 x 128k, Ext ROM : nil
	-	-	-	-	-	-	-	-	011	-	Ext SRAM : 16 x 64k, Ext ROM : nil
	-	-	-	-	-	-	-	-	100	-	Ext SRAM : nil, Ext ROM : present
	-	-	-	-	-	-	-	-	101	-	Ext SRAM : 8 x 64k, Ext ROM : present
	-	-	-	-	-	-	-	-	110	-	Ext SRAM : 8 x 128k, Ext ROM : present
	-	-	-	-	-	-	-	-	111	-	Ext SRAM : 16 x 64k, Ext ROM : present
Master Clock Source	-	-	-	-	-	-	-	-	-	0	Default
	-	-	-	-	-	-	-	-	-	1	When using circular buffer in the delta-sigma audio DAC

Note: MD4 and MD7 do not have any configuration assignment.

5. Memory Mappings

5.1 Memory Configuration

The memory configuration will make different kind of memory allocation. There are three kind of memory configuration. And notice that the Peripherals Configuration Registers and Embedded 56k byte address' A16 & A17 value depend on memory configuration.

56k byte embedded memory,
no external memory

Address A17 ~ A0	Mapping
00000 : 0DFFF	Embedded 56k byte
0E000 : 0EFFF	Reserved
0F000 : 0FFFF	Peripherals Configuration Registers
10000 : 1FFFF	Reserved (BLANK)
20000 : 2FFFF	Reserved (BLANK)
30000 : 3FFFF	Reserved (BLANK)

56k byte embedded memory,
64k byte external memory

Address A17 ~ A0	Mapping
00000 : 0FFFF	1 st 64k byte at CS0
10000 : 1DFFF	Embedded 56k byte
1E000 : 1EFFF	Reserved
1F000 : 1FFFF	Peripherals Configuration Registers
20000 : 2FFFF	Reserved (BLANK)
30000 : 3FFFF	Reserved (BLANK)

56k byte embedded memory,
128k byte external memory

Address A17 ~ A0	Mapping
00000 : 0FFFF	1 st 64k byte of the 128k byte at CS0
10000 : 1FFFF	2 nd 64kbyte of the 128k byte at CS0
20000 : 2DFFF	Embedded 56k byte
2E000 : 2EFFF	Reserved
2F000 : 2FFFF	Peripherals Configuration Registers
30000 : 3FFFF	Reserved (BLANK)

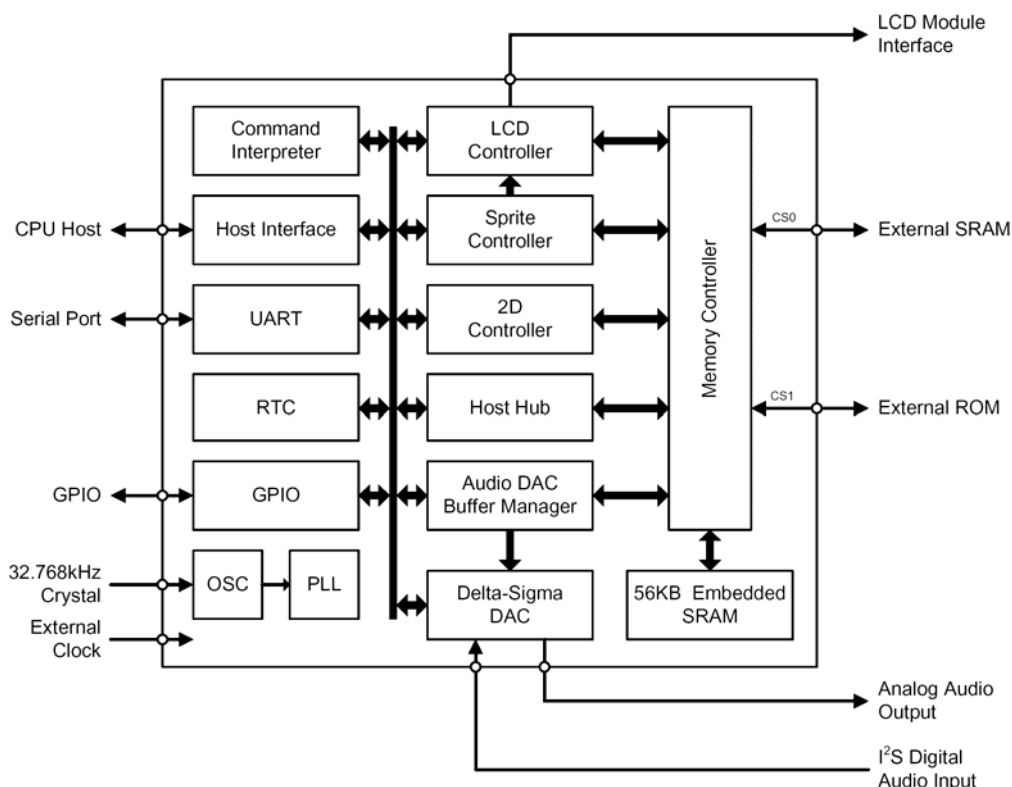
5.2 Memory Mapped Peripheral Configuration Registers

Address A15 ~ A0	Peripheral
F000 – F001	System Configuration – ID
F004 – F006	Command Interpreter
F010 – F07F	Reserved
F080 – F0FF	LCD Controller
F100 – F17F	Sprite / overlay Controller
F180 – F1FF	2D Hardware Acceleration Controller
F200 – F27F	GPIO
F280 – F2FF	Reserved
F300 – F4FF	Reserved
F500 – F57F	Memory Controller
F580 – FFFF	Reserved

Note: A16, A17 value depend on Memory Configuration, see the above section for details.

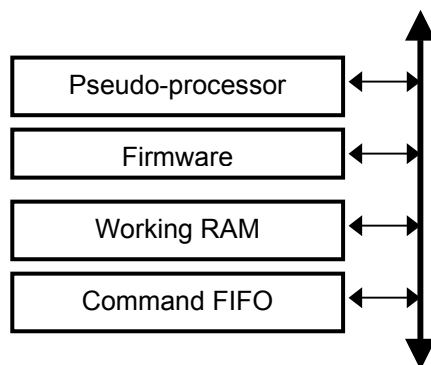
6. Function Specifications

6.1 Function Block



6.2 Command Interpreter

6.2.1 Command Interpreter Structure



The Pseudo-processor along with its associated Firmware and Working RAM is responsible for the interpretation of the commands that stored in the Command FIFO.

It executes the commands by setting the appropriate internal registers of the corresponding functional blocks (e.g. 2D hardware acceleration controller).

Except in RS232 serial host mode, the Command FIFO can store up to eight commands. Each command consists of 1 byte op-code and up to 64 bytes of parameters (data). In RS232 serial host mode, only one command can be stored in the Command FIFO with a maximum length of 65 bytes. Furthermore, there is no read back path for the Command Interpreter, i.e. it is a write only system. However in RS232 serial host mode, register content can be read back through the "Acknowledge Packet" (see Section 2.5 for details).

6.3 Command Packet Format

All commands are organized in packet with a 1 byte “Opcode” followed by optional parameters / data up to 64 bytes.

Sequence	Content
1	Opcode
2	Parameters / Data (up to 64bytes)
3	:
:	:

6.4 Opcode Description

6.4.1 Opcode Group

Opcode Value	Descriptions
00 - 0F	Reserved for Serial Communication
10 - 1F	Fonts Drawing Operations
20 - 2F	Geometric Drawing Operations
30 - 3F	Reserved
40 - 4F	Reserved
50 - 5F	Reserved
60 - 6F	Communication
70 - 7F	Reserved
80 - 8F	System Control
F0 - FF	Reserved for serial mode synchronization

6.5 Opcode Descriptions

Opcode (hex)	Operations	No of Parameters / Data (byte)	Parameters / Data
00	Set "Control & Status Port" of the Command Interpreter	1	The value of this data will be directly written to the Control & Status register.
10	charset_config	1	00: Built in 8x8 ASCII 01: 8x8 CGRAM (Embedded RAM) 02: 8x16 CGRAM (Embedded RAM) 03: 16x16 CGRAM (Embedded RAM) 04: 16x16 GB2312-80 (External ROM) 05: 16x16 BIG5 (External ROM) 06: 8x8 Custom 8-bit encoding (External ROM) 07: 8x8 Custom 16-bit encoding (External ROM)
12	set_print_coord	4	Character Print Coordinates x-coordinate (2-bytes) y-coordinate (2-bytes) * Mono LCD, x = (multiple of 8) – 1 * Color LCD, no restriction on the value of x coordinate
14	set_font_fgcolor	2	Character Foreground Color (same as td_fgcolor) * Mono LCD: 1bpp, 2bpp, 4bpp * Color LCD: 12-bit STN (4R:4G:4B)
15	set_font_bgcolor	2	Character Background Color * LCD: 1bpp, 2bpp, 4bpp * LCD: 12-bit STN (4R:4G:4B)
16	show_char	1 or 2	Display Character
17	show_string	1 + (1 to 63)	Display String No. of characters (1-byte) Character String (1 to 63-bytes)
19	define_CGRAM	1 + (1 to 32)	CGRAM Bitmap Character code (1 byte) Bitmap pattern (1 to 32 bytes)
20	td_fgcolor	2	Set Foreground Color *Mono LCD: 1bpp, 2bpp, 4bpp *Color LCD: 12-bit STN (4R:4G:4B)
23	draw_pixel	4	Draw Pixel x-coordinate (2-bytes) y-coordinate (2-bytes)
24	draw_line	8	Draw Line x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
26	draw_rect	8	Draw Hollow Rectangle (Box) x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
27	fill_rect	8	Fill Rectangle (Box) x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
28	draw_circle	5	Draw Circle x_center (2-bytes) y_center (2-bytes) radius (1-byte)
29	fill_circle	5	Fill Circle x_center (2-bytes) y_center (2-bytes) radius (1-byte)
60	set_baud	2	Set baud rate divisor (lower byte) divisor (upper byte)
80	refresh_setting	0	-
81	set_mem_ptr	3	Set memory pointer address (3-bytes)
82	read_reg	2	Read register(*ONLY used in RS232 serial host mode) address (2 bytes)
83	write_reg	2 + 1	Write register address (2-bytes) data (1-byte)
84	write_mem	1 + (1 to 63)	Write memory No. of data (1 byte) data (1 to 63 bytes)
8F	clk_en	6	Enable memory clock; [69, 45, 61, 67, 6C, 65 (6-bytes in hex)]

6.6 RS232 Serial Host Communication Packet Format

In RS232 serial host mode, each communication packet starts with a byte of “FF” and ended with “FE”. Length of parameters (one byte) is also required to be embedded into the packet. An Acknowledge Packet will be sent back to the RS232 serial host by the T8000 once the command is finished execution.

RS232 Serial host Communication Packet Format

Sequence	No of byte	Content
1	1	0xFF (hex)
2	1	Opcode
3	1	Length of Parameters
4	1 to 64	Parameters / Data (up to 64bytes)
5	1	0xFE (hex)

Note: A “FF” bytes sequence of length equal to or more than 65 will cause re-synchronization.

RS232 Serial host re-synchronization Packet Format

Sequence	No of byte	Content
1	1	0xFF (hex)
2	1	0xFF (hex)
3	More than 65	0xFF (hex)

For commands required read data (Opcode 82) from the T8000, it will send read data embedded in the Acknowledge Packet automatically when data is ready.

RS232 Serial host Acknowledge Packet Format, without “register read data”

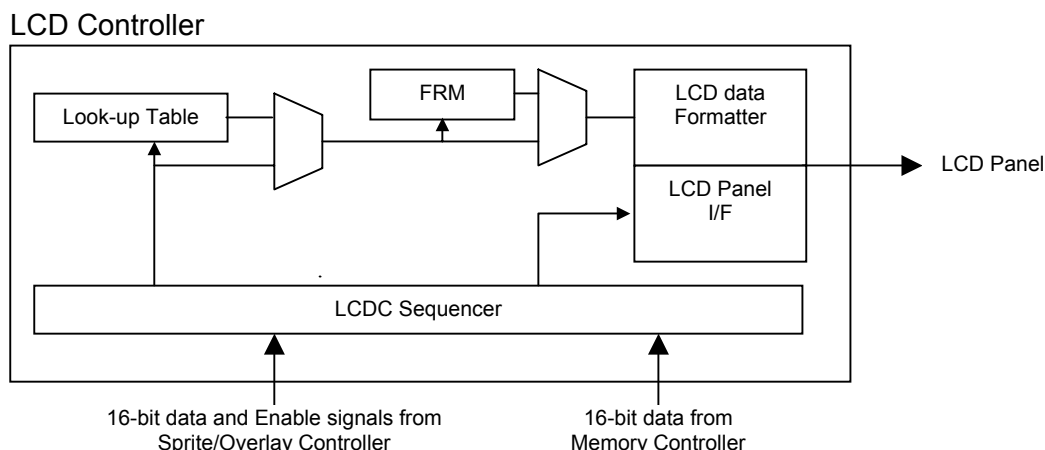
Sequence	No of byte	Content
1	1	0x00 (hex)

RS232 Serial host Acknowledge Packet Format, with “register read data”

Sequence	No of byte	Content
1	1	Register read data
2	1	0x00 (hex)

7. LCD Controller

7.1 LCD Controller Structure



The LCD Controller consists of five modules

1. LCDC Sequencer

The LCDC Sequencer controls the data flow either from the Sprite Controller or the Memory Controller to the Look-up Table or the FRM. It also generates the display refresh addresses to be sent to the Memory Controller.

2. FRM (Frame Rate Modulator)

A FRM produces 16 different levels of shade out of 4 bit input data. In Monochrome STN panel mode, one FRM output will be used to support 16 simultaneous gray levels. In Color STN panel mode, there are three FRMs to produce 3 sets (R-G-B) of 16 levels of shade to support 4096 simultaneous colors. These outputs are then passed to the LCD Data Formatter.

3. LCD Data Formatter

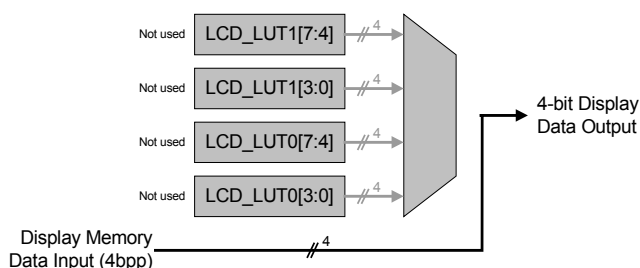
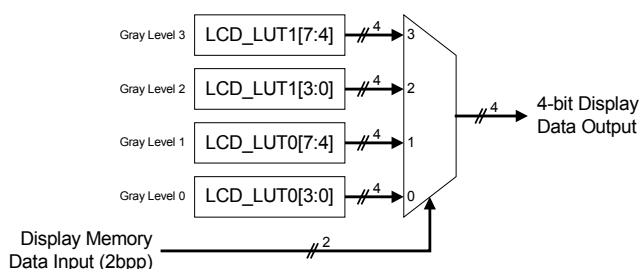
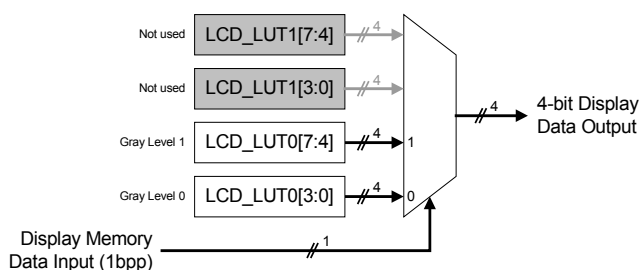
According to different panel type, the Formatter packs and shifts the incoming data and directs them out to the connected LCD panel.

4. LCD Panel Interface

According to different panel type, The Panel Interface generates the necessary signals to drive the connected panel.

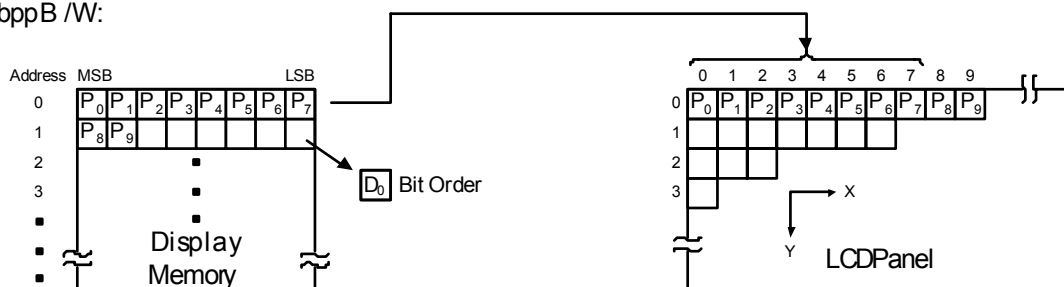
5. Look-up Table

There is a 4x4 look-up table for the translation of pixel data read from the display memory to display data output in 1 bit-per-pixel and 2 bit-per-pixel modes. In 4 bit-per-pixel and color modes, the look-up table is shut down and the pixel data is piped out as display data.

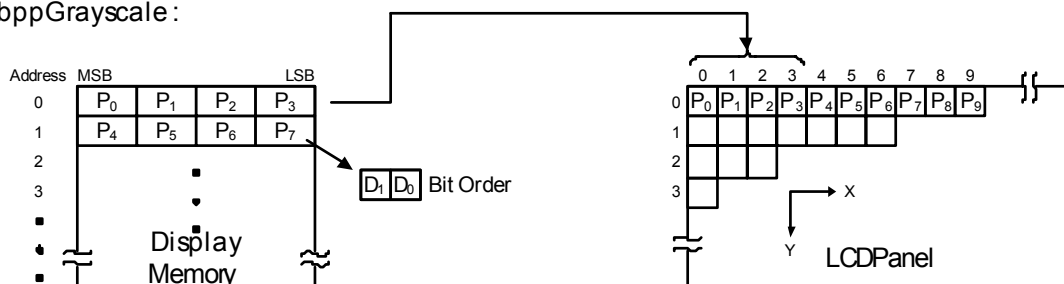


7.2 Display Data Format

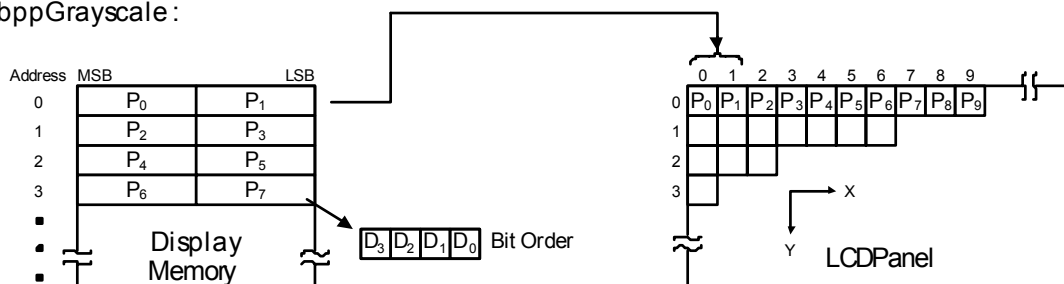
1-bppB /W:



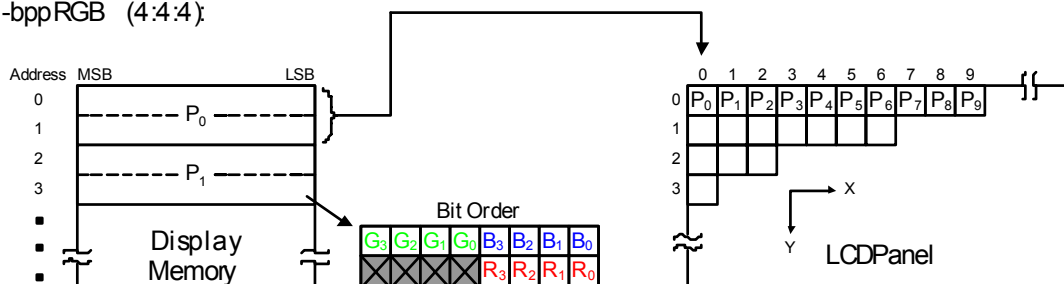
2-bppGrayscale :



4-bppGrayscale :

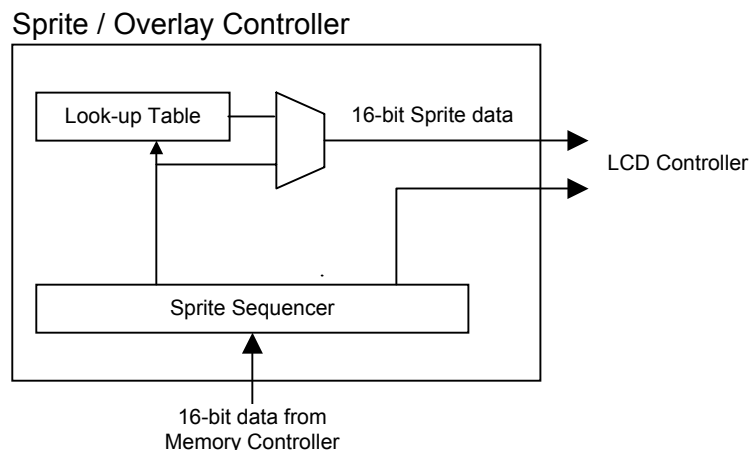


12-bppRGB (4:4:4):



7.3 Sprite / Overlay Controller

A small image, which is overlaid on a background picture, is called “sprite”. A sprite may consist of a sequence of images. Viewers can experience animation effect if the sequence of images is loaded to screen continually. Moreover, the sprite image colors can be changed at anytime through the built-in look-up table.



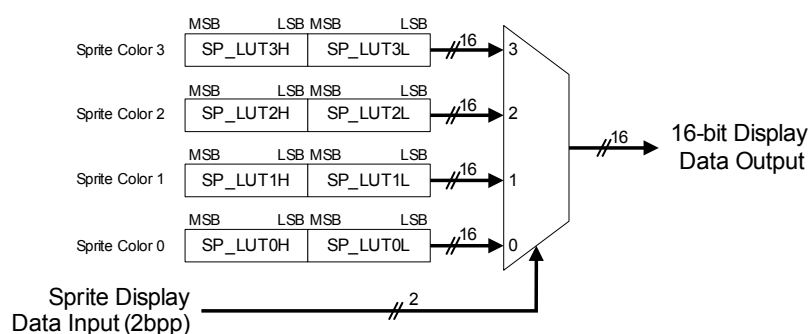
The Sprite Controller consists of two modules

1. Sprite Sequencer

The Sprite Sequencer controls the data flow read from the Memory Controller to either the Look-up Table, then to the LCD Controller or directly to the LCD Controller. It also generates the Enable signal to be sent to the LCD Controller and the Sprite refresh addresses to be sent to the Memory Controller.

2. Look-up Table

There is a 4x16 look-up table for the translation of Sprite data (2 bits) read from the memory and output (16 bits) to the LCD Controller. When Enable signal is high, these data bits will be passed to the LCD Data Formatter. When Enable signal is low, the data bits from the LCD Sequencer will be used instead.



7.4 2D Hardware Acceleration Controller

The 2D Hardware Acceleration Controller has two drawing engines. They are geometry drawing engine and font drawing engine. All drawing functions must be initiated through the Command Interpreter except the read back of foreground color and background color.

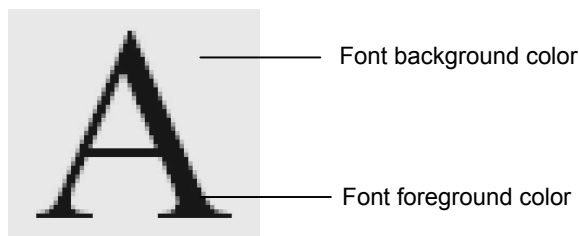
Geometry Drawing Engine

The Geometry Drawing Engine will perform line draw, circle draw, circle draw with solid fill, box draw and box draw with solid fill by using the assigned foreground color.

Font Drawing Engine

According to the input character code, the Font Drawing Engine will first read the corresponding font bitmap data either from the internal font data area or from an external ROM/flash and then rendering the character on the LCD screen with color expansion. Color expansion is the mapping of the font bitmap data (1bpp) to a different (target) color depth system. The supported target color depth of T8000 is 2bpp, 4bpp and 12bpp (CSTN). The supported character formats are ASCII, user-defined custom encoding RAM (CGRAM), GB2312-80, BIG5 and user-defined custom encoding ROM. The supported font sizes are 8x8, 8x16 and 16x16.

The Font Drawing Engine uses both the foreground color and background color.

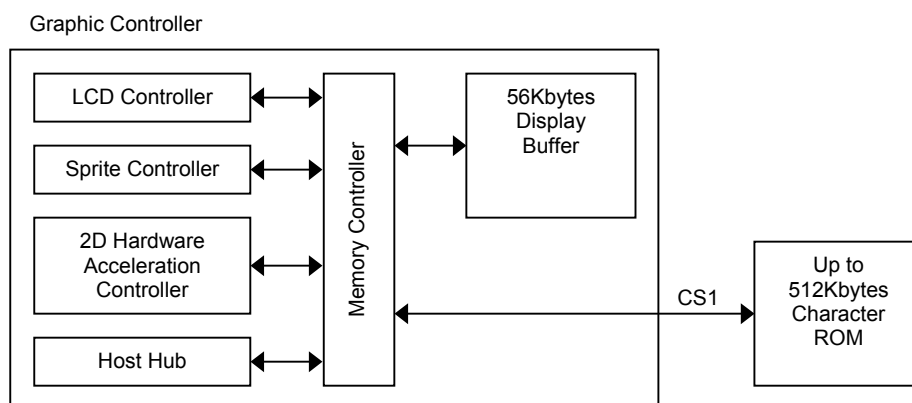


7.5 Memory Controller

The Memory Controller arbitrates between four input modules, LCD Controller, Sprite Controller, 2D Hardware Acceleration Controller, and two memory devices, 56Kbytes embedded Display Buffer and up to 512Kbytes of external ROM/Flash. It also generates the necessary signals to interface with these memory devices.

In general, the first 52Kbytes of the 56Kbytes embedded Display Buffer serves as display memory and sprite/overlay memory. The other 4Kbytes of Display Buffer holds the internal ASCII font data and user-defined custom encoding font data.

Furthermore, a ROM/flash with size up to 512Kbytes can be connected to the T8000 (CS1) to serve as the font data bitmap storage. This storage can hold up to 16,000 16x16 Chinese characters.



7.6 Host Hub

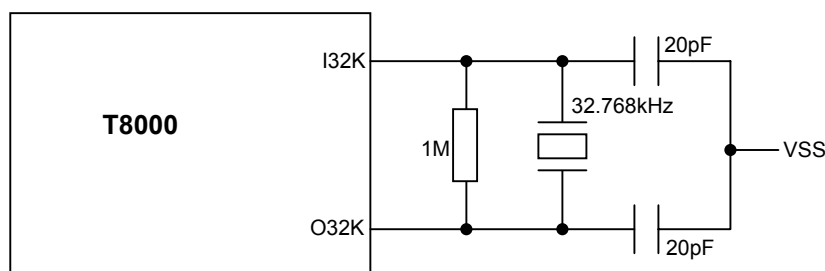
Host Hub acts as a communication bridge between the Host Interface and the Memory Controller.

7.7 GPIO

There are two GPIO pins can be used by the host to perform various control task.

7.8 OSC and PLL

The value of the crystal oscillator is 32.768KHz. This clock source would enable the internal PLL to generate all the necessary operating clocks to different internal modules. The operating memory clock (MCLK) frequency is 24MHz and the operating pixel clock frequency would be divided from this memory clock. The pixel clock is either auto-set by the T8000 during power-up or by the host through the LCD Controller register.



7.9 Registers Settings

7.9.1 System Configuration Registers

Address (hex) A15 ~ A0	R/W	Reset Value	Descriptions
F000	Read / Write	1000 0000	Chip ID Port, Always read back 80 (hex) for T8000 Write "DE FC 0B" (hex) to enable memory clock, same as command with OPCODE "8F".
F001	Read	0000 0000	Chip Revision Port, Always read back 00 (hex) for T8000
F004	Write	-	Command Packet Port - Writing of Command Packets.
F006	Write	xxx1 xxx0	Port for writing control or reading status Bit[7:5] : Reserved Bit[4] : DISPLAY ON / OFF 0=DISPLAY ON 1=DISPLAY OFF Bit[3:1] : Reserved Bit[0] : End of Command, Write "1" after each command packet
	Read	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : FIFO full Read "1" if Command FIFO is full. Hosts must read this bit = "0" before writing to Command Packet Port.
F080	Read / Write	0000 0000	Bit[7:4] : Reserved Bit[3] : STN Panel I/F Data Width 0=4-bit single 1=8-bit single Bit[2] : Color Mode Select 0=Monochrome 1=Color Bit[1:0] : Color Depth Select If Monochrome (Bit[2]=0) 00=1 bit-per-pixel 01=2 bit-per-pixel 10=4 bit-per-pixel 11=Reserved If Color (Bit[2] = 1) 01=12 bit-per-pixel (CSTN panel) 00=Reserved 10=Reserved 11=Reserved
F081	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Panel Horizontal Character Count – 1, Panel Horizontal Character Count[8:0] supports horizontal panel size up to 128 characters or 1024 pixels.
F082	Read / Write	0000 0000	Bit[7:0] : Panel Line Count - 1 bit[7:0]
F083	Read / Write	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : Panel Line Count – 1 bit[8], Panel Line Count[8:0] supports vertical panel size up to 512 lines.
F084	Read / Write	0000 0000	Bit[7:0] : Display Start Position X Coordinate – bit[7:0]
F085	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position X Coordinate – bit[9:8]
F086	Read / Write	0000 0000	Bit[7:0] : Display Start Position Y Coordinate – bit[7:0]
F087	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position Y Coordinate – bit[9:8]
F088	Read / Write	0000 0000	LCD_LUT1 Bit[7:4] : for Gray level 3 Bit[3:0] : for Gray level 2
F089	Read / Write	0000 0000	LCD_LUT0 Bit[7:4] : for Gray level 1 Bit[3:0] : for Gray level 0
F08A	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Virtual Display Character count – 1 It supports horizontal virtual size up to 128 characters or 1024 pixels.
F08B	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : WF count for STN panels 000000=WF pin toggles every frame 000001=WF pin toggles every 2 LP pulses 000010=WF pin toggles every 3 LP pulses : 111111=WF pin toggles every 64 LP pulses



F08C	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Horizontal non-display period 0000=2 characters (16 pixels) 0001=3 characters (24 pixels) : 1111=17 characters (136 pixels)
F08D	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Vertical non-display period 0000: 1 line 0001: 2 lines : 1111: 16 lines
F08E	Read / Write	0000 000x	Bit[7:4] : Pixel Clock Divider 0000=24 MHz (divided by 1) 0001=12 MHz (divided by 2) 0010=8 MHz (divided by 3) 0011=6MHz (divided by 4) : 1111=1.5MHz (divided by 16) Bit[3] : Display Blank 0=Normal 1=Blank Bit[2] : Display Invert 0=Normal 1=Invert Bit[1] : LCD_ON Polarity 0=LCD_ON pin active low 1=LCD_ON pin active high Bit[0] : Reserved
F08F	Read /Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Number of frames to start – 1 (Maximum 128 frames)
F090	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Front Porch for TFT panels 000000=1 pixel 000001=2 pixels : 111111=64 pixels
F091	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Back Porch for TFT panels 000000=1 pixel 000001=2 pixels : 111111=64 pixels
F092	Read /Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Horizontal Pulse Width for TFT panels 00000=1 pixel 00001=2 pixels : 11111=32 pixels
F093	Read /Write	0000 0000	Bit[7:0] : Scratch Pad register
F094	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Front Porch for TFT panels 000000=1 line 000001=2 lines : 111111=64 lines
F095	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Back Porch for TFT panels 000000: 1 line 000001: 2 lines : 111111: 64 lines
F096	Read /Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Vertical Pulse Width for TFT panels 00000: 1 line 00001: 2 lines : 11111: 32 lines



F100	Read /Write	00xx xx00	Bit[7] : Enable / Disable 0=Disable Sprite 1=Enable Sprite Bit[6] : Transparency 0=Transparency disable 1=Transparency enable When enabled: Sprite data = 00 becomes transparent and LCD background will be displayed instead. Bit[5:2] : Reserved Bit[1:0] : Sprite Modes Select 00=reserved 01=Sprite with 2 bit-per-pixel 10=reserved 11=reserved
F102	Read /Write	0000 0000	Bit[7:0] : SP_LUT0L[7:0]
F103	Read / Write	0000 0000	Bit[7:0] : SP_LUT0H[7:0]
F104	Read / Write	0000 0000	Bit[7:0] : SP_LUT1L[7:0]
F105	Read / Write	0000 0000	Bit[7:0] : SP_LUT1H[7:0]
F106	Read / Write	0000 0000	Bit[7:0] : SP_LUT2L[7:0]
F107	Read / Write	0000 0000	Bit[7:0] : SP_LUT2H[7:0]
F108	Read / Write	0000 0000	Bit[7:0] : SP_LUT3L[7:0]
F109	Read / Write	0000 0000	Bit[7:0] : SP_LUT3H[7:0]
F10A	Read / Write	0000 0000	Bit[7:0] : Sprite Horizontal Pixel Count – 1 Maximum 256 pixels
F10B	Read / Write	0000 0000	Bit[7:0] : Sprite Vertical Line Count – 1 Maximum 256 lines
F10C	Read / Write	0000 0000	Bit[7:0] : Sprite Horizontal Start Position bit[7:0]
F10D	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Sprite Horizontal Start Position bit[9:8] Sprite Horizontal Start Position bit[9:0] is measured in pixels and counted from left to right of the edge of the panel display (i.e. not virtual display).
F10E	Read / Write	0000 0000	Bit[7:0] : Sprite Vertical Start Position bit[7:0]
F10F	Read / Write	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : Sprite Vertical Start Position bit[8] Sprite Vertical Start Position bit[8:0] is measured in lines and counted from top to bottom of the edge of the panel display (i.e. not virtual display).
F142	Write Only	0000 0000	Bit[7:0] : Sprite / overlay storage starting address bit[7:0]
F143	Write Only	0000 0000	Bit[7:0] : Sprite / overlay storage starting address bit[15:8]
F144	Write Only	0000 0000	Bit[7:2] : Reserved Bit[1:0] : Sprite / overlay storage starting address bit[17:16] This is the starting address to put the sprite/overlay image
F180	Read Only	0000 0000	Bit[7:0] : Background Color bit[7:0]
F181	Read Only	0000 0000	Bit[7:0] : Background Color bit[15:8]
F182	Read Only	0000 0000	Bit[7:0] : Foreground Color bit[7:0]
F183	Read Only	0000 0000	Bit[7:0] : Foreground Color bit[15:8]
F500	Read / Write	1110 1110	CS0 Configuration Port - Pulse Width Bit[7:4] : Write Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001=2 memory clocks : 1110=15 memory clocks 1111=Reserved Bit[3:0] : Read Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks : 1110:15 memory clocks 1111: Reserved



F501	Read / Write	0000 0000	CS0 Configuration Port - Control <u>Bit[7]</u> : Enable bit 0=Disable CS0 1=Enable CS0 <u>Bit[6]</u> : Memory data bus width 0=8-bit memory data bus width 1=16-bit memory data bus width <u>Bit[5]</u> : 16-bit SRAM option 0=two 8-bit SRAMs 1=one 16-bit SRAM <u>Bit[4]</u> : Reserved <u>Bit[3]</u> : CS0 assertion time relative to address assertion. 0=CS0 and address assert at the same time 1=CS0 lags address by 1 memory clock. <u>Bit[2]</u> : CS0 Negation Timing 0=CS0 and Address negate at the same time 1=CS0 leads Address by 1 memory clock in write access. <u>Bit[1]</u> : Write Enable Assertion Time 0=Write Enable and Address Assert at the same time. 1=Write Enable lags Address by 1 memory clock. <u>Bit[0]</u> : Write Enable Negation Time 0=Write Enable and Address negate at the same time. 1=Write Enable leads Address by 1 memory clock.
F504	Read / Write	Bit[3:0] = 1110	CS1 Configuration Port - Pulse Width <u>Bit[7:4]</u> : Reserved <u>Bit[3:0]</u> : Read Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001=2 memory clocks 0010=3 memory clocks : 1101=14 memory clocks 1110=15 memory clocks 1111=Reserved
F505	Read / Write	0000 0000	CS1 Configuration Port - Control <u>Bit[7]</u> : Enable bit 0=Disable CS1 1=Enable CS1 <u>Bit[6]</u> : Memory data bus width 0=8-bit memory data bus width 1=16-bit memory data bus width <u>Bit[5]</u> : Reserved <u>Bit[4]</u> : Reserved <u>Bit[3]</u> : CS1 assertion time relative to address assertion. 0=CS1 and Address assert at the same time 1=CS1 lags Address by 1 memory clock. <u>Bit[2]</u> : CS1 Negation Timing 0=CS1 and Address negate at the same time 1=CS1 leads Address by 1 memory clock in write access. <u>Bit[1:0]</u> : Reserved
F6C4	Read / Write	xx11 0011	Set Memory Clock Divide <u>Bit[7:6]</u> = Reserved <u>Bit[5:0]</u> = 010000 to set 24MHz memory clock for proper operations

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage (*1)	H_{VDD}	-0.3	+5.5	V	$V_{SS} = 0V$ (*1)
Supply Voltage (*2)	L_{VDD}	-0.3	+5.5	V	$V_{SS} = 0V$ (*2)
Input Voltage	V_I	-0.3	$H_{VDD}+0.5$	V	$V_{SS} = 0V$
Input Voltage (*3)	V_{I5V}	-0.3	5.5	V	$V_{SS} = 0V$
Output Voltage	V_O	-0.3	$H_{VDD}+0.5$	V	$V_{SS} = 0V$
Operating Temperature	T_{OP}	-30	+85	°C	No Condensation
Storage Temperature	T_{ST}	-65	150	°C	No Condensation

Note:

*1 H_{VDD} includes VDD_{IO} and VDD_{AUDIO} .

*2 L_{VDD} includes VDD_{CORE} and VDD_{PLL} .

*3 V_{I5V} is for 5V tolerance inputs.

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

8.2 Recommended Operating Conditions

Items	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	H_{VDD}	3.0	3.3	3.6	V
Supply Voltage	L_{VDD}	2.3	2.5	2.7	V
Input Voltage	V_I	V_{SS}	-	H_{VDD}	V
Operation Temperature	T_{OP}	-20	25	70	°C

8.3 DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	CMOS level, $H_{VDD} = 3.6V$	2.2	-	-	V
Low Level Input Voltage	V_{IL}	CMOS level, $H_{VDD} = 3.0V$	-	-	0.8	V
Positive Trigger Voltage	V_{T+}	CMOS Schmitt	1.4	-	2.7	V
Negative Trigger Voltage	V_{T-}	CMOS Schmitt	0.6	-	1.8	V
Input Leakage Current	I_{LI}	-	-5	-	5	uA
Input Pin Capacitance	C_I	$f = 1MHz$, $H_{VDD} = 0V$	-	-	8	pF
Pull Down Resistance	R_{PD}	$V_I = H_{VDD}$	60	120	240	KΩ
High Level Output Voltage	V_{OH}	$I_{OH} = -3mA$ (Type 1) $I_{OH} = -6mA$ (Type 2) $I_{OH} = -12mA$ (Type 3)	$H_{VDD}-0.4$	-	-	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 3mA$ (Type 1) $I_{OL} = 6mA$ (Type 2) $I_{OL} = 12mA$ (Type 3)	-	-	0.4	V
Output leakage Current	I_{LO}	-	-5	-	5	uA
Output Pin Capacitance	C_O	$f = 1MHz$, $H_{VDD} = 0V$	-	-	8	pF
Bi-directional Pin Capacitance	C_{IO}	$f = 1MHz$, $H_{VDD} = 0V$	-	-	8	pF

8.4 AC Characteristics

8.4.1 Host Interface - Write Timing

Symbol	Parameter	Min	Max	Unit
t_{OHZ}	Output Disable to Data Output in High-Z	0	8	ns
t_{WAIT}	Write (nWE) Assertion to Wait (nWAIT) Assertion	0	9	ns
t_{AS}	Address Setup Time	9	-	ns
t_{WP}	Write Pulse Width	$2 \cdot T$	-	ns
t_{CW}	Chip Select Assertion to Write Assertion	0	-	ns
t_{WC}	Write Negation to Chip Select Negation	0	-	ns
t_{WR}	Write Recovery Time	T	-	ns
t_{DS}	Write Data to Write Assertion Setup	0	-	ns
t_{DH}	Write Data to Write Negation Hold	0	-	ns

Note:

T = Memory Clock period (default setting is 24MHz or 41.6 nsec)

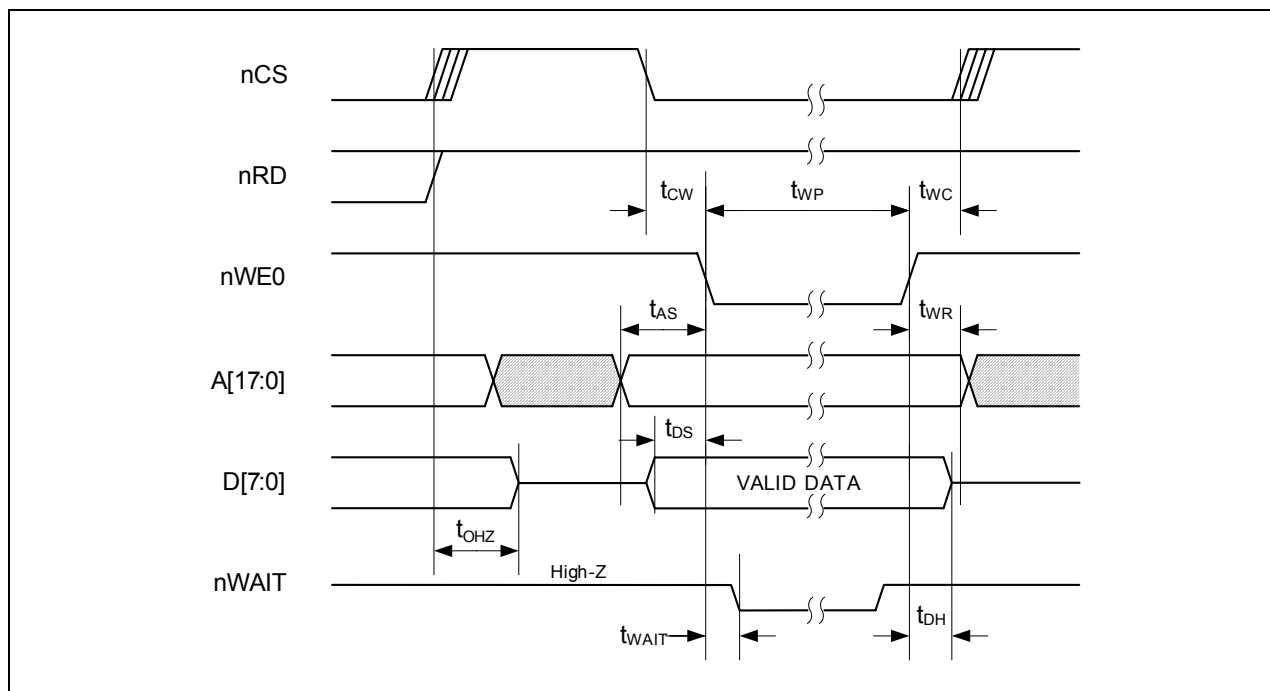
$H_{VDD} = 3.0V \pm 10\%$,

$L_{VDD} = 2.5V \pm 10\%$,

$T_{OP} = -40^{\circ}C - 85^{\circ}C$

T_{RISE} and T_{FALL} for all inputs must be ≤ 5 nsec (10% - 90%)

Output Loading = 20 pF on all interface



Host Interface - Write Timing Diagram

8.4.2 Host Interface – Read Timing

Symbol	Parameter	Min	Max	Unit
t_{CR}	Chip Select Assertion to Read Assertion	0	-	ns
t_{RC}	Read Negation to Chip Select Negation	0	-	ns
t_{AS}	Address Setup Time	9	-	ns
t_{RP}	Read Pulse Width	$2 \cdot T$	-	ns
t_{AH}	Address Hold Time to Read Negation	T	-	ns
t_{OLZ}	Read to Output in Low-Z	3	-	ns
t_{AC}	Access Time	-	11	ns
t_{WAIT}	Read (nRD) Assertion to Wait (nWAIT) Assertion	0	9	ns
t_{WDS}	Valid Data before nWAIT Negation	10	-	ns
t_{OHZ}	Output Disable to Data Output in High-Z	0	8	ns

Note:

T = Memory Clock period (default setting is 24MHz or 41.6 nsec)

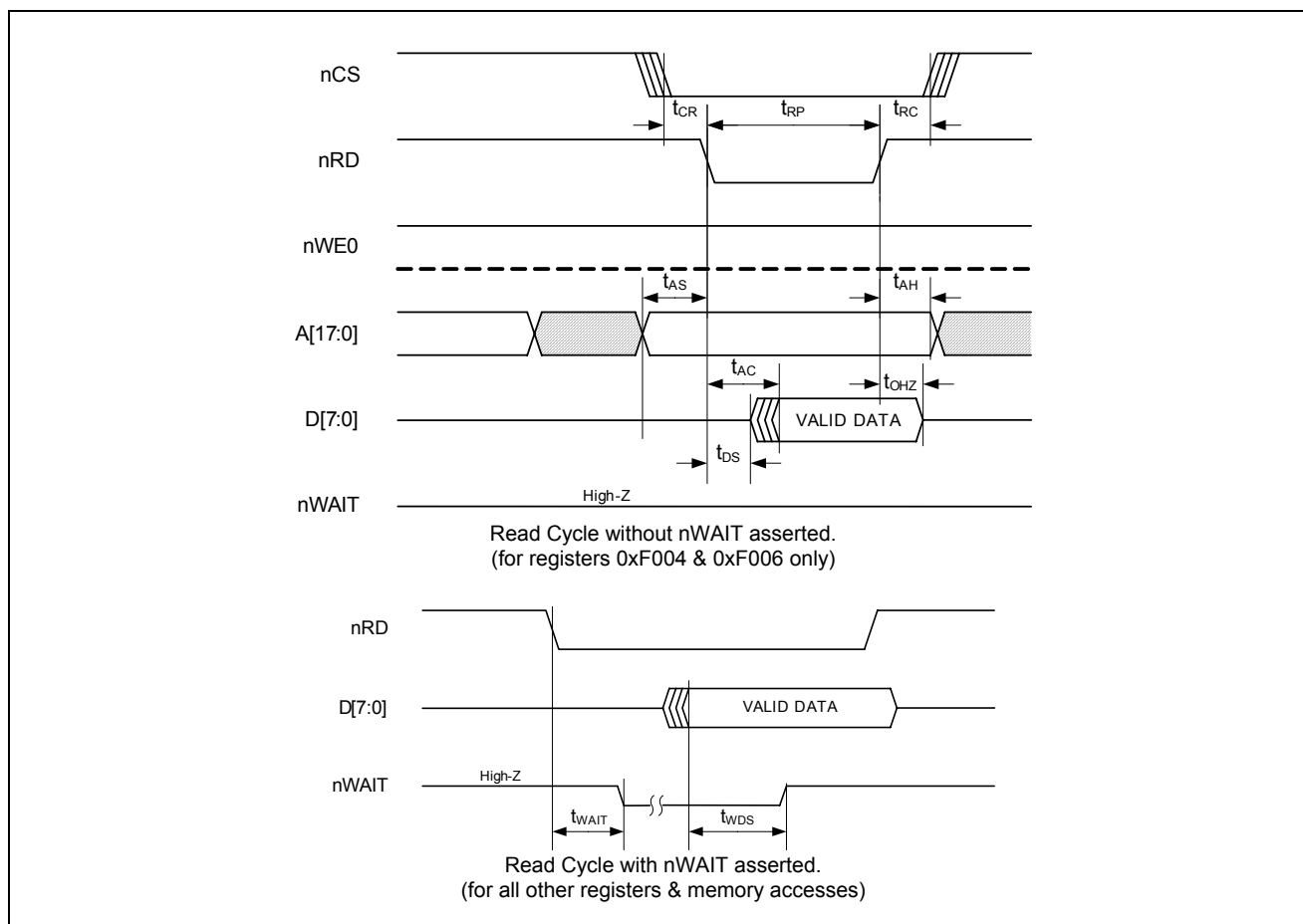
$H_{VDD} = 3.0V \pm 10\%$,

$L_{VDD} = 2.5V \pm 10\%$,

$T_{OP} = -40^{\circ}C - 85^{\circ}C$

T_{RISE} and T_{FALL} for all inputs must be ≤ 5 nsec (10% - 90%)

Output Loading = 20 pF on all interface



Host Interface Read Timing

8.4.3 Memory Interface - Write Timing

Symbol	Parameter	Min	Max	Unit
t_{WC}	Valid Write Address Cycle	38	46	ns
t_{SA}	Address Valid to Chip Select Assertion	-4	0	ns
t_C	Active Chip Select Cycle	40	42	ns
t_{HA}	Chip Select Negation to Address Invalid	-2	0	ns
t_{AW}	Address Valid to Write End	11	16	ns
t_{WP}	Write Pulse Width	10	-	ns
t_{AD}	Address Valid to Data Valid	-	6	ns
t_{LZA}	Address Valid to Low-Z	0	6	ns
t_{WD}	Write Negation to Data Invalid	11	-	ns
t_{HZA}	Address to High-Z	0	5	ns
t_{BA}	Address Valid to Byte Enable Assertion	-5	0	ns
t_{BN}	Byte Enable Negation to Address Invalid	-3	0	ns

Note:

T = Memory Clock period (default setting is 24MHz or 41.6 nsec)

waitwr = Register "0xF500" bit[7:4] (nMCS0)

csat = Register "0xF501" bit[3] (nMCS0)

csnt = Register "0xF501" bit[2] (nMCS0)

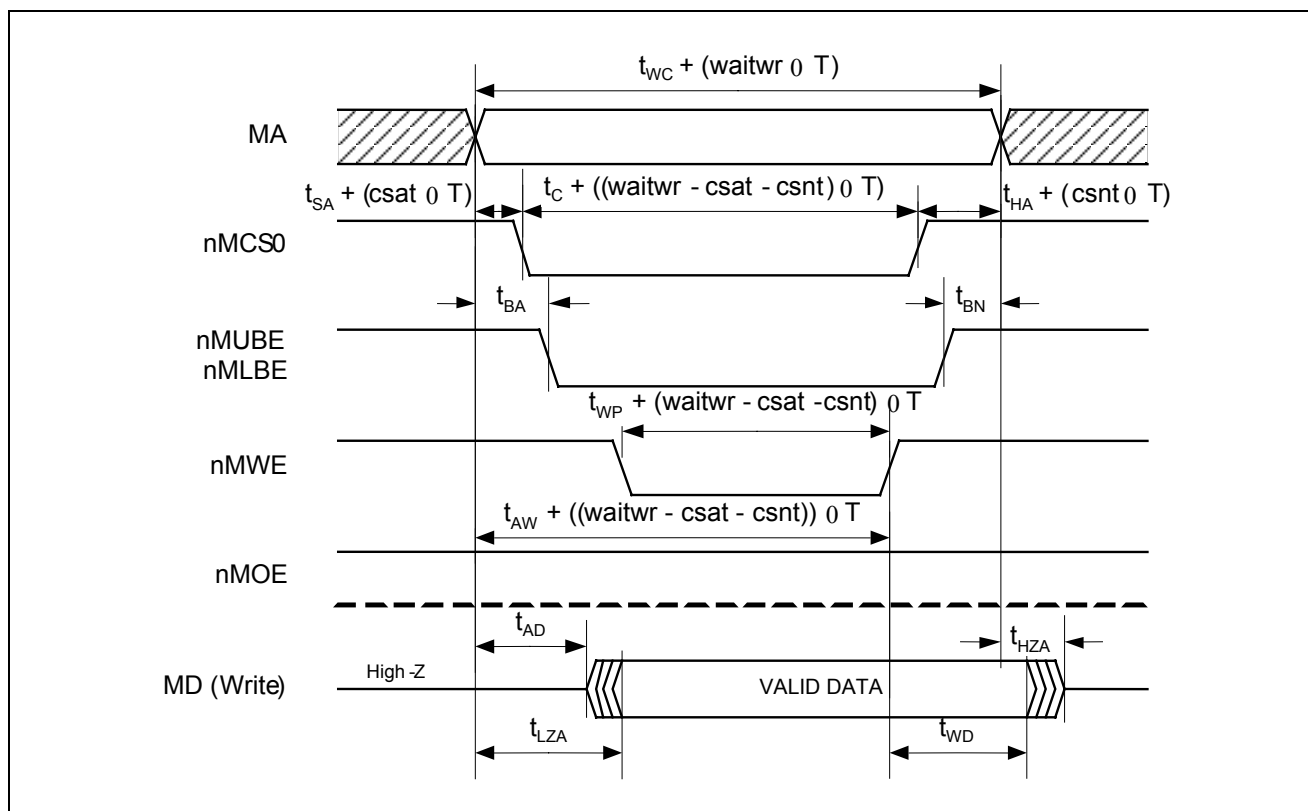
$H_{VDD} = 3.0V \pm 10\%$,

$L_{VDD} = 2.5V \pm 10\%$,

$T_{OP} = -40^{\circ}C - 85^{\circ}C$

T_{RISE} and T_{FALL} for all inputs must be ≤ 5 nsec (10% - 90%)

Output Loading = 20 pF on all interface



Memory Interface Write Timing

8.4.4 Memory Interface - Read Timing

Symbol	Parameter	Min	Max	Unit
t_{WC}	Valid Write Address Cycle	38	46	ns
t_{SA}	Address Valid to Chip Select Assertion	-4	0	ns
t_C	Active Chip Select Cycle	40	42	ns
t_{HA}	Chip Select Negation to Address Invalid	-2	0	ns
t_{SO}	Output Enable Assertion to Address Valid	-4	0	ns
t_{HO}	Output Enable Negation to Address Invalid	-2	0	ns
t_{SD}	Data Setup	6	-	ns
t_{HD}	Data Hold	0	-	ns
t_{BA}	Address Valid to Byte Enable Assertion	-5	0	ns
t_{BN}	Byte Enable Negation to Address Invalid	-3	0	ns

Note:

T = Memory Clock period (default setting is 24MHz or 41.6 nsec)

NMCSx = Either nMCS0 or nMCS1

waitrd = Register "0xF500" bit[3:0] (nMCS0) or Register "0xF504" bit[3:0] (nMCS1)

csat = Register "0xF501" bit[3] (nMCS0) or Register "0xF505" bit[3] (nMCS1)

csnt = Register "0xF501" bit[2] (nMCS0) or Register "0xF505" bit[2] (nMCS1)

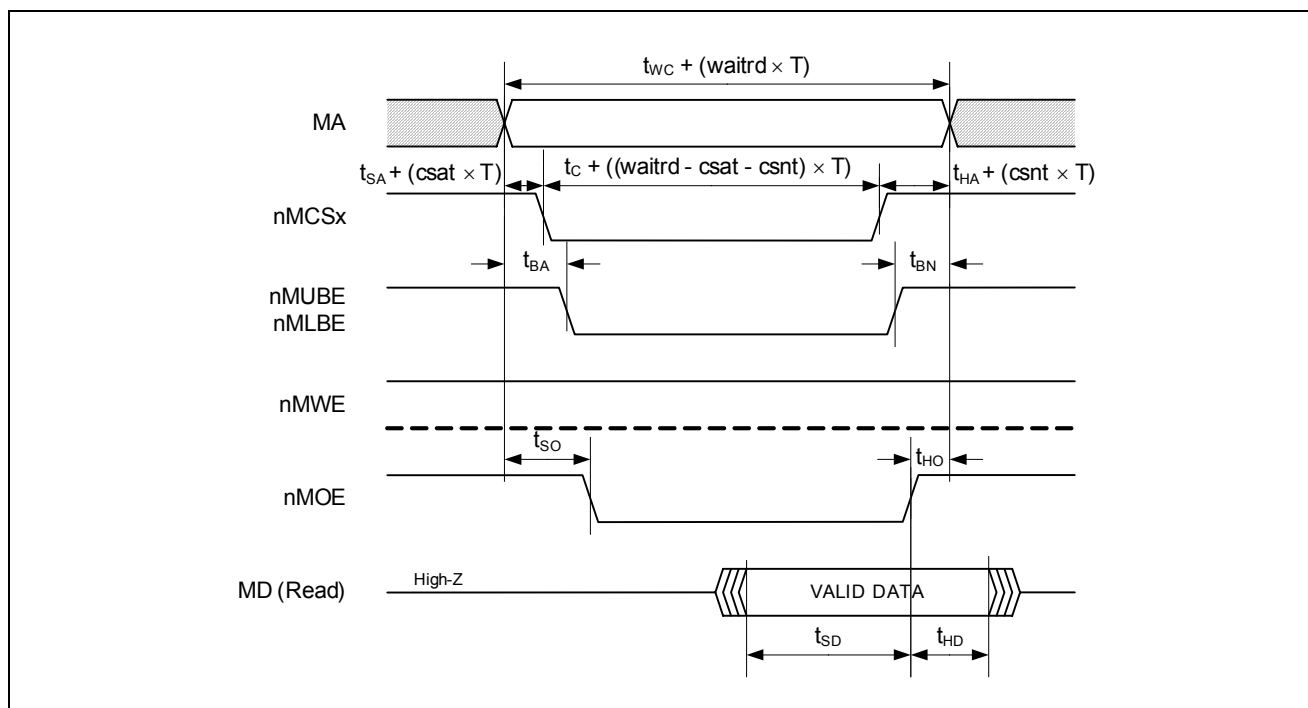
$H_{VDD} = 3.0V \pm 10\%$,

$L_{VDD} = 2.5V \pm 10\%$,

$T_{OP} = -40^{\circ}C - 85^{\circ}C$

T_{RISE} and T_{FALL} for all inputs must be ≤ 5 nsec (10% - 90%)

Output Loading = 20 pF on all interface



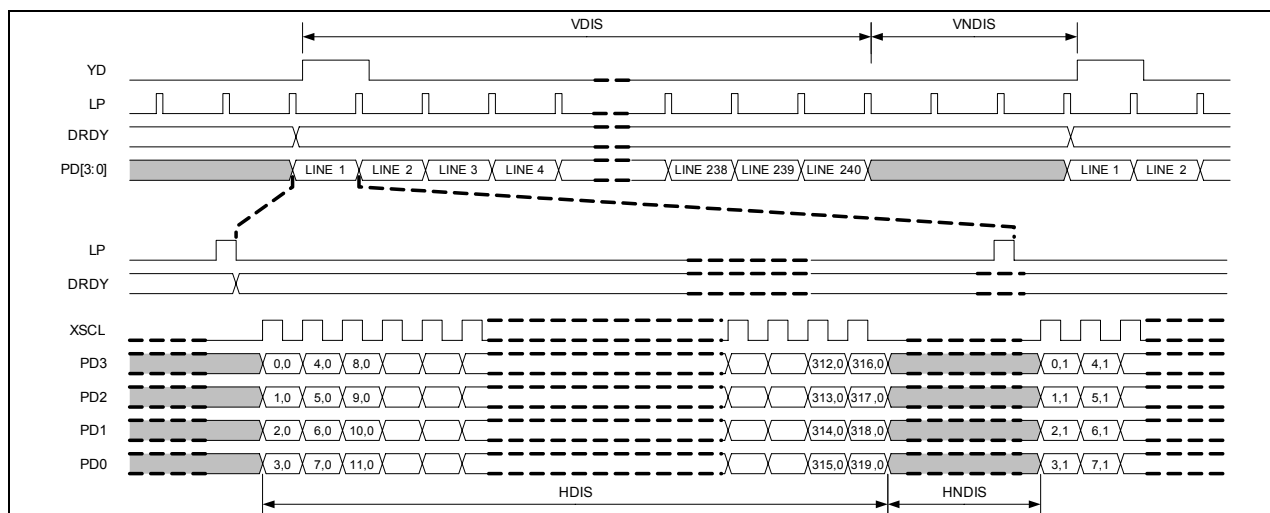
Memory Interface Read Timing

8.4.5 LCD Panel Interface - 4-bit Single Monochrome STN Panel Timing

Symbol	Parameter	Min	Max	Unit
t_1	YD setup to LP falling edge	$t_3 - t_2$		ns
t_2	YD hold from LP falling edge	$2 \times \text{Ptime} - 2$		ns
t_3	LP period	$\text{HDIS} + \text{HNDIS} - 2$		ns
t_4	LP pulse width	$8 \times \text{Ptime} - 2$		ns
t_5	DRDY (WF) changes state from LP rising edge	2		ns
t_6	XSCL falling edge to LP rising edge	$4 \times \text{Ptime} - 2$		ns
t_7	XSCL falling edge to LP falling edge	$12 \times \text{Ptime} - 5$		ns
t_8	LP falling edge to XSCL falling edge	$8 \times \text{Ptime} - 2$		ns
t_9	XSCL period	$4 \times \text{Ptime} - 2$		ns
t_{10}	XSCL "low" pulse width	$2 \times \text{Ptime} - 2$		ns
t_{11}	XSCL "high" pulse width	$2 \times \text{Ptime} - 2$		ns
t_{12}	PD[3:0] setup to XSCL falling edge	$2 \times \text{Ptime} - 5$		ns
t_{13}	PD[3:0] hold from XSCL falling edge	$2 \times \text{Ptime} + 2$		ns
t_{14}	LP falling edge to XSCL rising edge	$6 \times \text{Ptime} - 2$		ns

Note:

Ptime = Pixel clock period



Note:

VDIS=Vertical Display Period=<Register "0xF083" bit[0] & "0xF082" bit[7:0]> + 1 lines

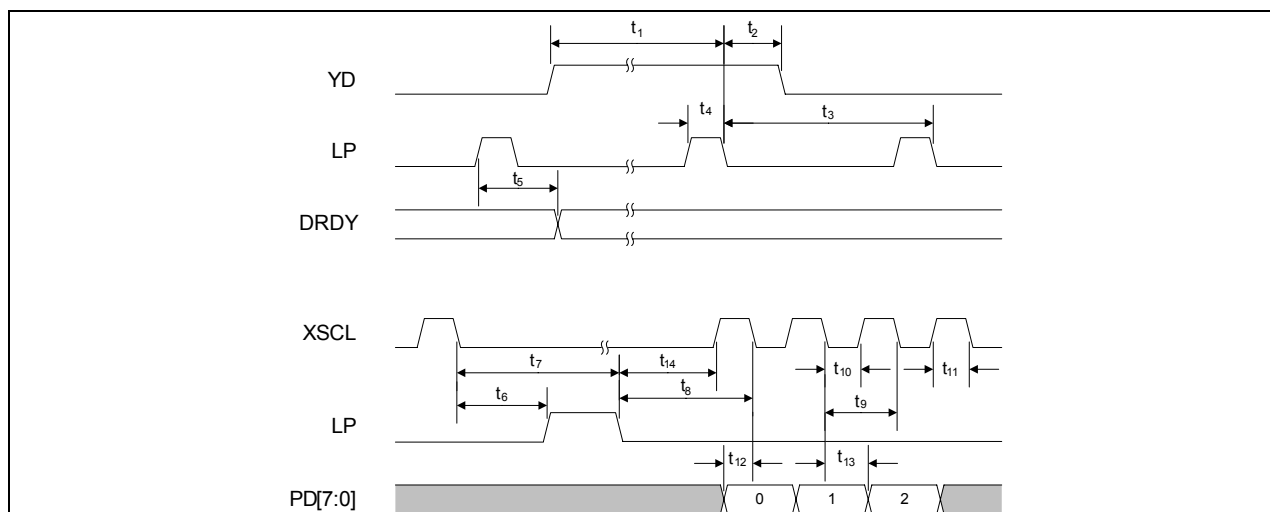
VNDIS=Vertical Non-display Period=<Register "0xF08D" bit[3:0]> + 1 lines

HDIS=Horizontal Display Period=<Register "0xF082" bit[6:0] + 1> * 8 * Pixel Clock period

HNDIS=Horizontal Non-display Period=<Register "0xF08C" bit[3:0] + 2> * 8 * Pixel Clock period

Pixel Clock is defined in Register "0xF08E" bit[7:4]

4-bit Single Monochrome STN Panel Timing Diagram

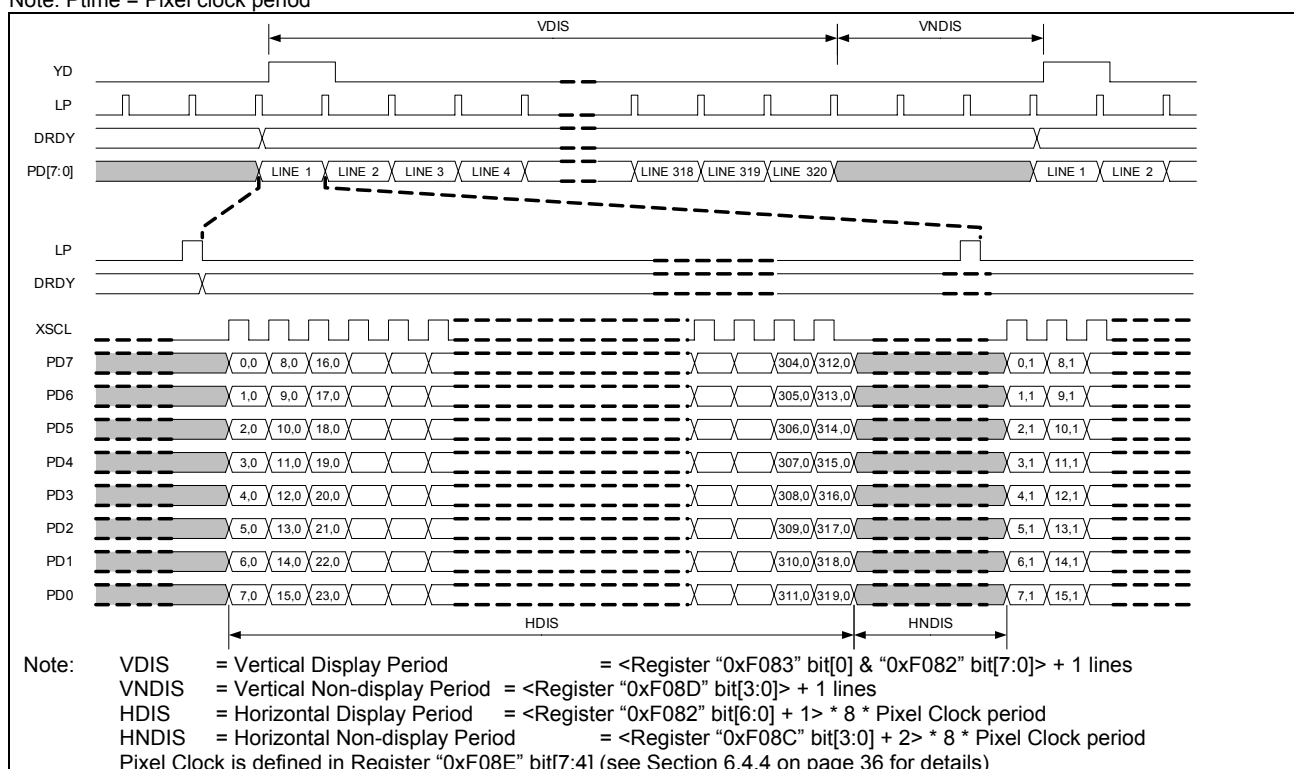


4-bit Single Monochrome STN Panel A.C. Timing Diagram

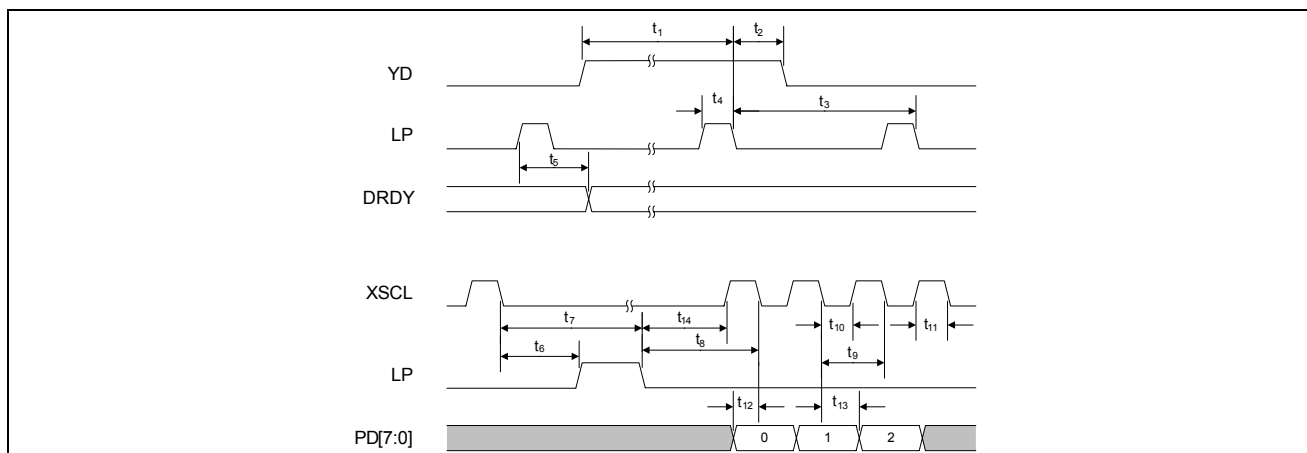
8.4.6 LCD Panel Interface - 8-bit Single Monochrome STN Panel Timing

Symbol	Parameter	Min	Max	Unit
t_1	YD setup to LP falling edge	$t_3 - t_2$		ns
t_2	YD hold from LP falling edge	$2 \times Ptime - 2$		ns
t_3	LP period	$HDIS + HNDIS - 2$		ns
t_4	LP pulse width	$8 \times Ptime - 2$		ns
t_5	DRDY (WF) changes state from LP rising edge	2		ns
t_6	XSCL falling edge to LP rising edge	$2 \times Ptime - 2$		ns
t_7	XSCL falling edge to LP falling edge	$10 \times Ptime - 5$		ns
t_8	LP falling edge to XSCL falling edge	$14 \times Ptime - 2$		ns
t_9	XSCL period	$8 \times Ptime - 2$		ns
t_{10}	XSCL "low" pulse width	$4 \times Ptime - 2$		ns
t_{11}	XSCL "high" pulse width	$4 \times Ptime - 2$		ns
t_{12}	PD[7:0] setup to XSCL falling edge	$4 \times Ptime - 5$		ns
t_{13}	PD[7:0] hold from XSCL falling edge	$4 \times Ptime + 2$		ns
t_{14}	LP falling edge to XSCL rising edge	$10 \times Ptime - 2$		ns

Note: Ptime = Pixel clock period



8-bit Single Monochrome STN Panel Timing

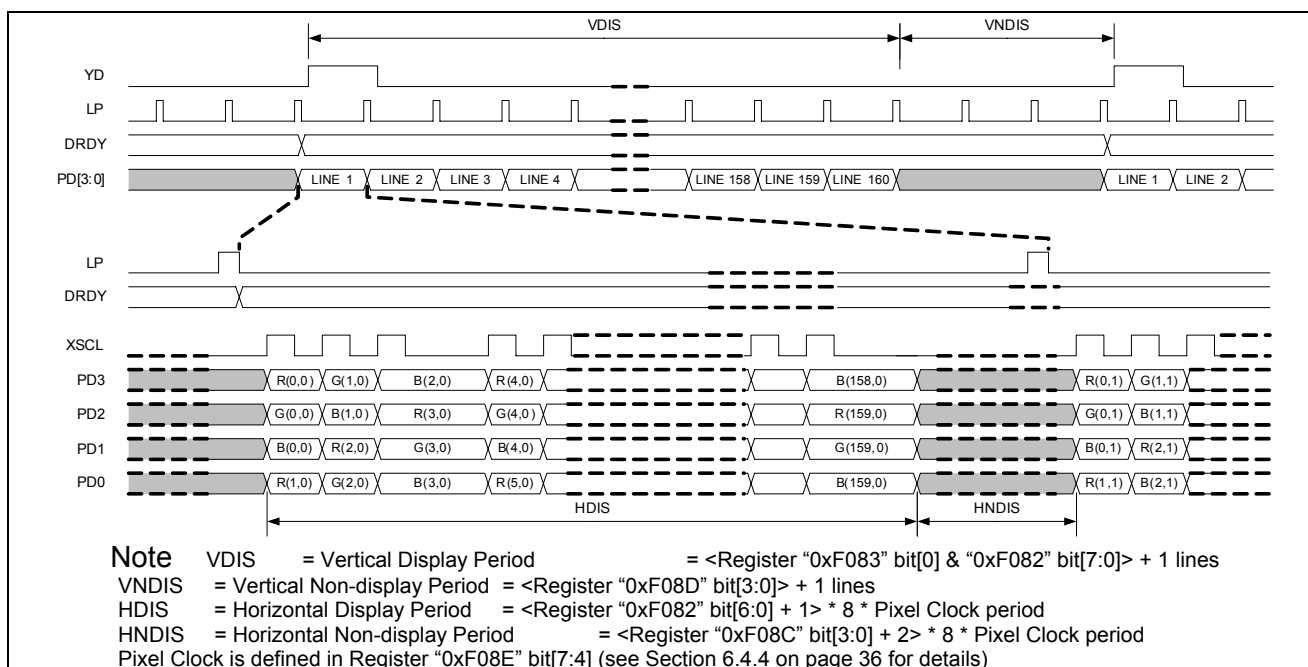


8-bit Single Monochrome STN Panel A.C. Timing

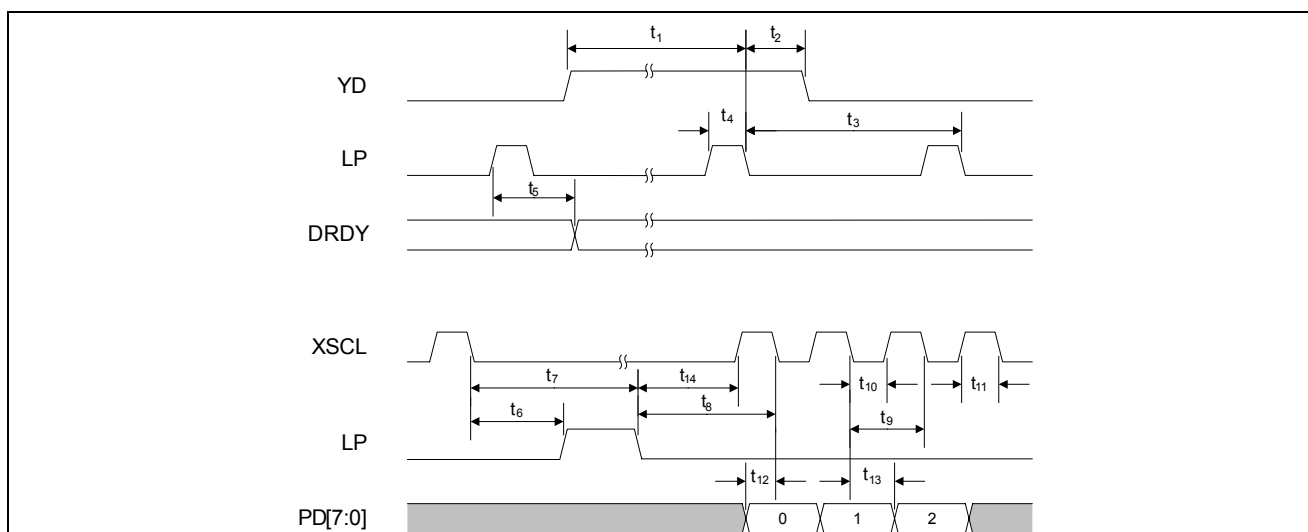
8.4.7 LCD Panel Interface - 4-bit Single Color STN Panel Timing

Symbol	Parameter	Min	Max	Unit
t_1	YD setup to LP falling edge	$t_3 - t_2$		ns
t_2	YD hold from LP falling edge	$2 * Ptime - 2$		ns
t_3	LP period	$HDIS + HNDIS - 2$		ns
t_4	LP pulse width	$8 * Ptime - 2$		ns
t_5	DRDY (WF) changes state from LP rising edge	2		ns
t_6	XSCL falling edge to LP rising edge	$3.5 * Ptime - 2$		ns
t_7	XSCL falling edge to LP falling edge	$11.5 * Ptime - 5$		ns
t_8	LP falling edge to XSCL falling edge	$6.5 * Ptime - 2$		ns
t_9	XSCL period	$Ptime - 2$		ns
t_{10}	XSCL "low" pulse width	$Ptime/2 - 2$		ns
t_{11}	XSCL "high" pulse width	$Ptime/2 - 2$		ns
t_{12}	PD[3:0] setup to XSCL falling edge	$Ptime/2 - 5$		ns
t_{13}	PD[3:0] hold from XSCL falling edge	$Ptime/2 + 2$		ns
t_{14}	LP falling edge to XSCL rising edge	$6 * Ptime - 2$		ns

Note: Ptime = Pixel clock period



4-bit Single Color STN Panel Timing

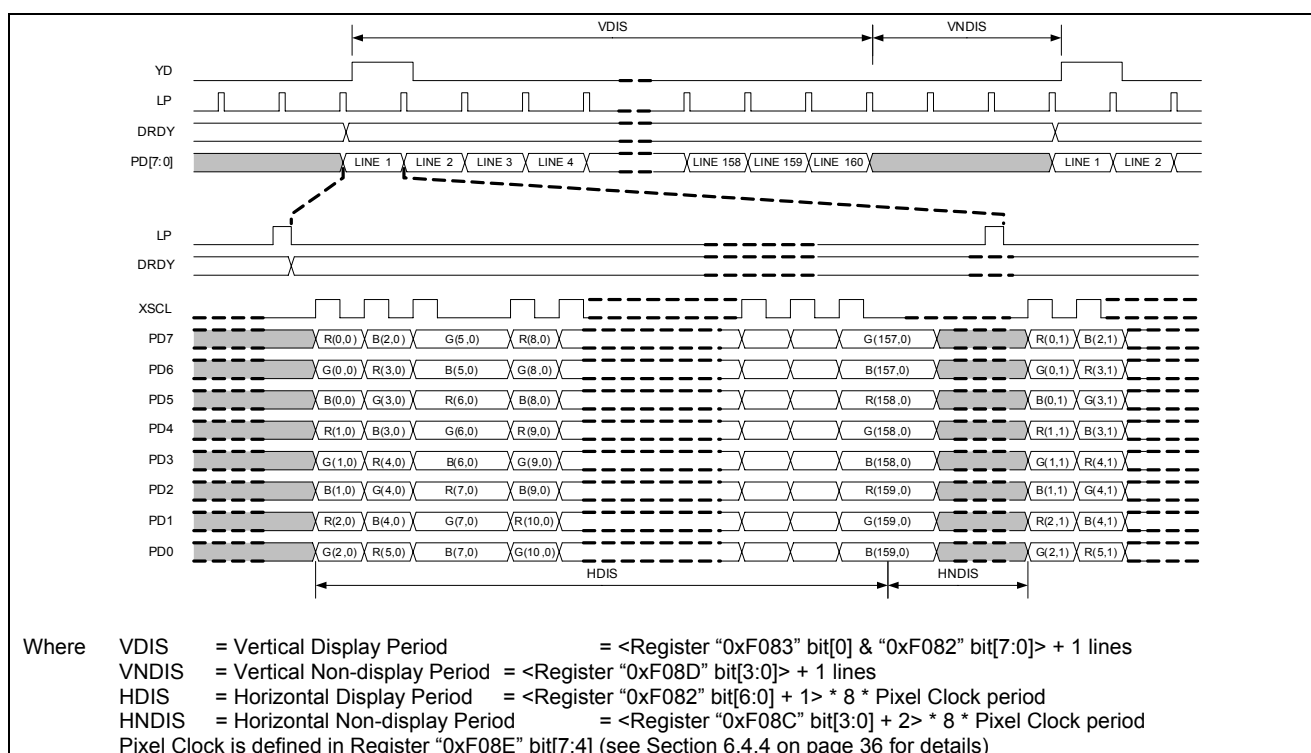


4-bit Single Color STN Panel A.C. Timing

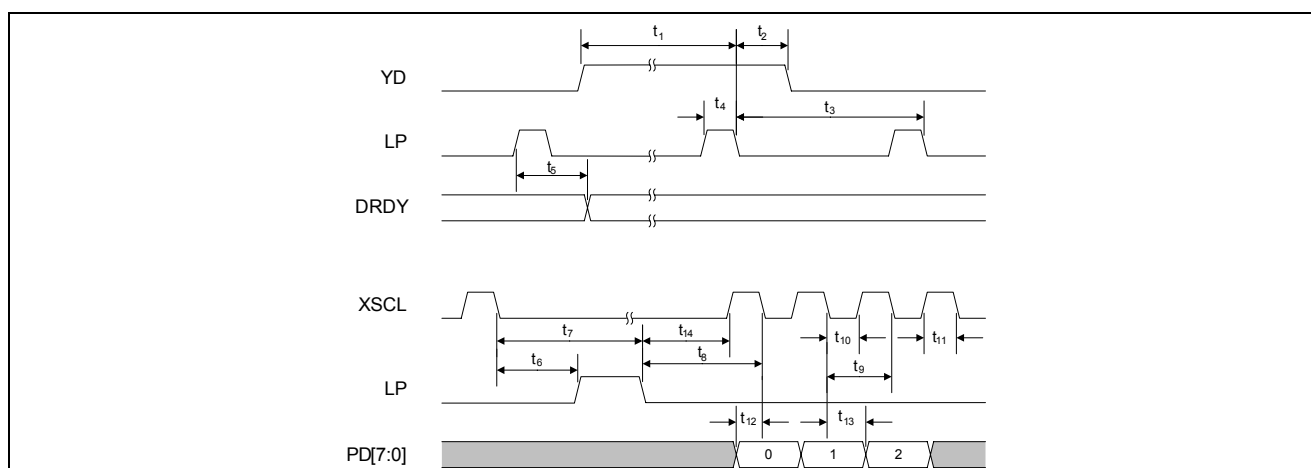
8.4.8 LCD Panel Interface - 8-bit Single Color STN Panel Timing

Symbol	Parameter	Min	Max	Unit
t_1	YD setup to LP falling edge	$t_3 - t_2$		ns
t_2	YD hold from LP falling edge	$2 * Ptime - 2$		ns
t_3	LP period	$HDIS + HNDIS - 2$		ns
t_4	LP pulse width	$8 * Ptime - 2$		ns
t_5	DRDY (WF) changes state from LP rising edge	2		ns
t_6	XSCL falling edge to LP rising edge	$Ptime - 2$		ns
t_7	XSCL falling edge to LP falling edge	$9 * Ptime - 5$		ns
t_8	LP falling edge to XSCL falling edge	$11 * Ptime - 2$		ns
t_9	XSCL period	$2 * Ptime - 2$		ns
t_{10}	XSCL "low" pulse width	$Ptime - 2$		ns
t_{11}	XSCL "high" pulse width	$Ptime - 2$		ns
t_{12}	PD[7:0] setup to XSCL falling edge	$Ptime - 5$		ns
t_{13}	PD[7:0] hold from XSCL falling edge	$Ptime + 2$		ns
t_{14}	LP falling edge to XSCL rising edge	$10 * Ptime - 2$		ns

Note: Ptime = Pixel clock period



8-bit Single Color STN Panel Timing



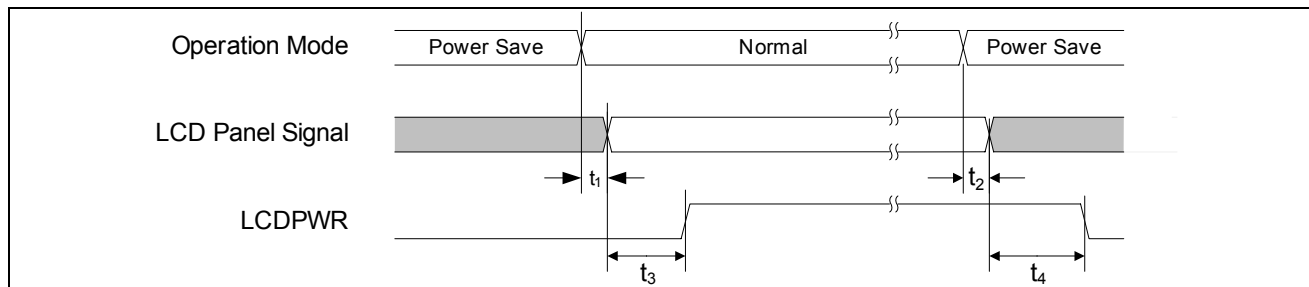
8-bit Single Color STN Panel A.C. Timing

8.5 Power Save Mode

Power Save mode, register "0xF006" bit[3] = 1. (Hardware reset default value)

Normal operating mode, register "0xF006" bit[3] = 0.

8.5.1 LCDPWR Pin Sequence when Entering / Exiting Power Save mode



LCDPWR (LCD_ON Pin) Sequence Timing

Symbol	Parameter	Min	Max	Unit
t ₁	Exit Power Save mode to LCD panel signals active	0		Frames
t ₂	Enter Power Save mode to LCD panel signals inactive	0		Frames
t ₃	LCD panel signal active to LCD_ON pin active	0	128	Frames
t ₄	LCD panel signal inactive to LCD_ON pin inactive	3		Frames

Timing of t₃ is programmed through register "0xF08F" bit[6:0], and the default value of t₃ is 128 frames.

Furthermore, the active state (polarity) of the LCD_ON pin can be programmed through register "0xF08E" bit[1]. Default LCD_ON pin polarity is active low.

8.5.2 Power Consumption

As a reference, Table 2.6 below shows the power consumption of the T8000 when connecting to a 320x240 monochrome LCD panel.

Items	Power Consumption (current in mA)
IO	1.4
CORE	9.2
CORE (Power Save)	0.85

Conditions :
IO VDD = 3.3V,
CORE VDD = 2.5V,
4 bit-per-pixel,
Pixel Clock = 6MHz
Memory Clock = 24MHz



9. Revision Note

Rev.	Descriptions	Release Date
0.1	Preliminary Release	2006-10-03